FIG. 1

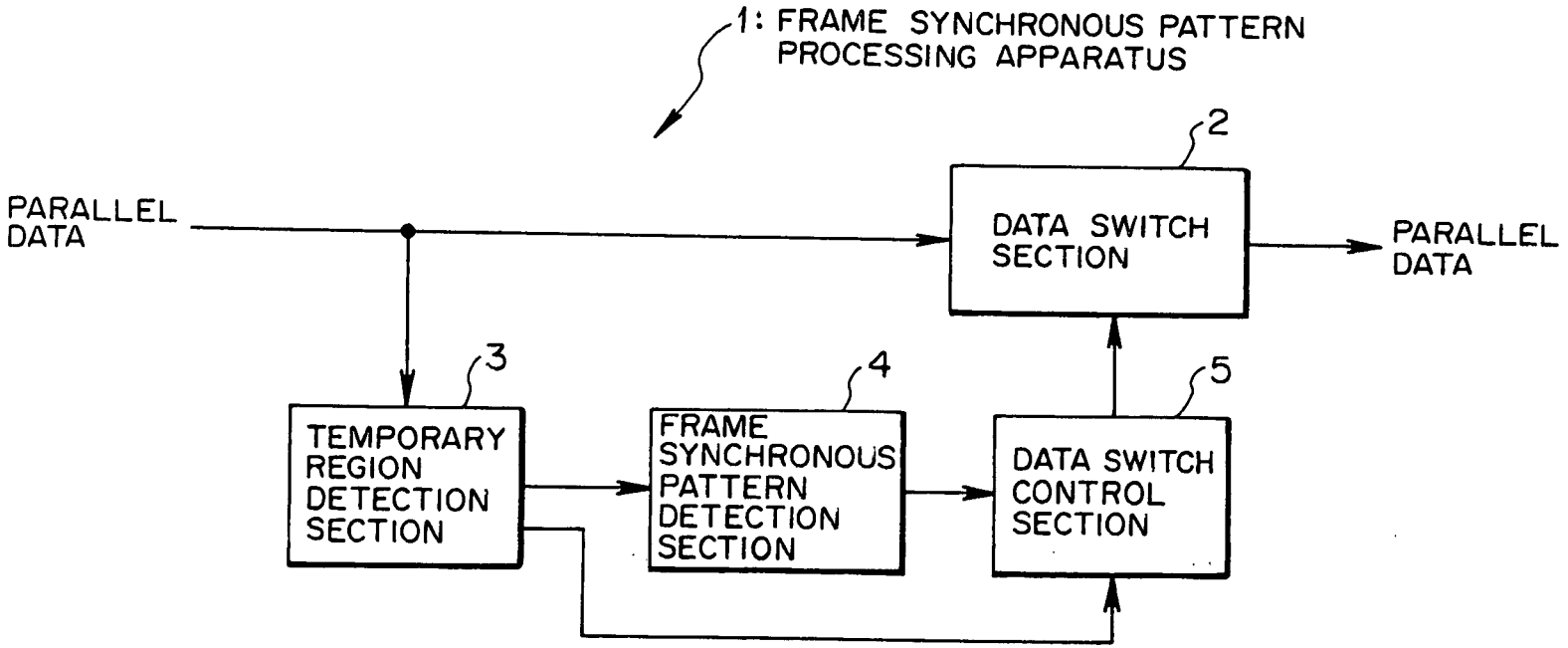

1: FRAME SYNCHRONOUS PATTERN PROCESSING APPARATUS
2
PARALLEL DATA
DATA SWITCH SECTION
PARALLEL DATA
3
4
5
TEMPORARY REGION DETECTION SECTION
FRAME SYNCHRONOUS PATTERN DETECTION SECTION
DATA SWITCH CONTROL SECTION

FIG. 2

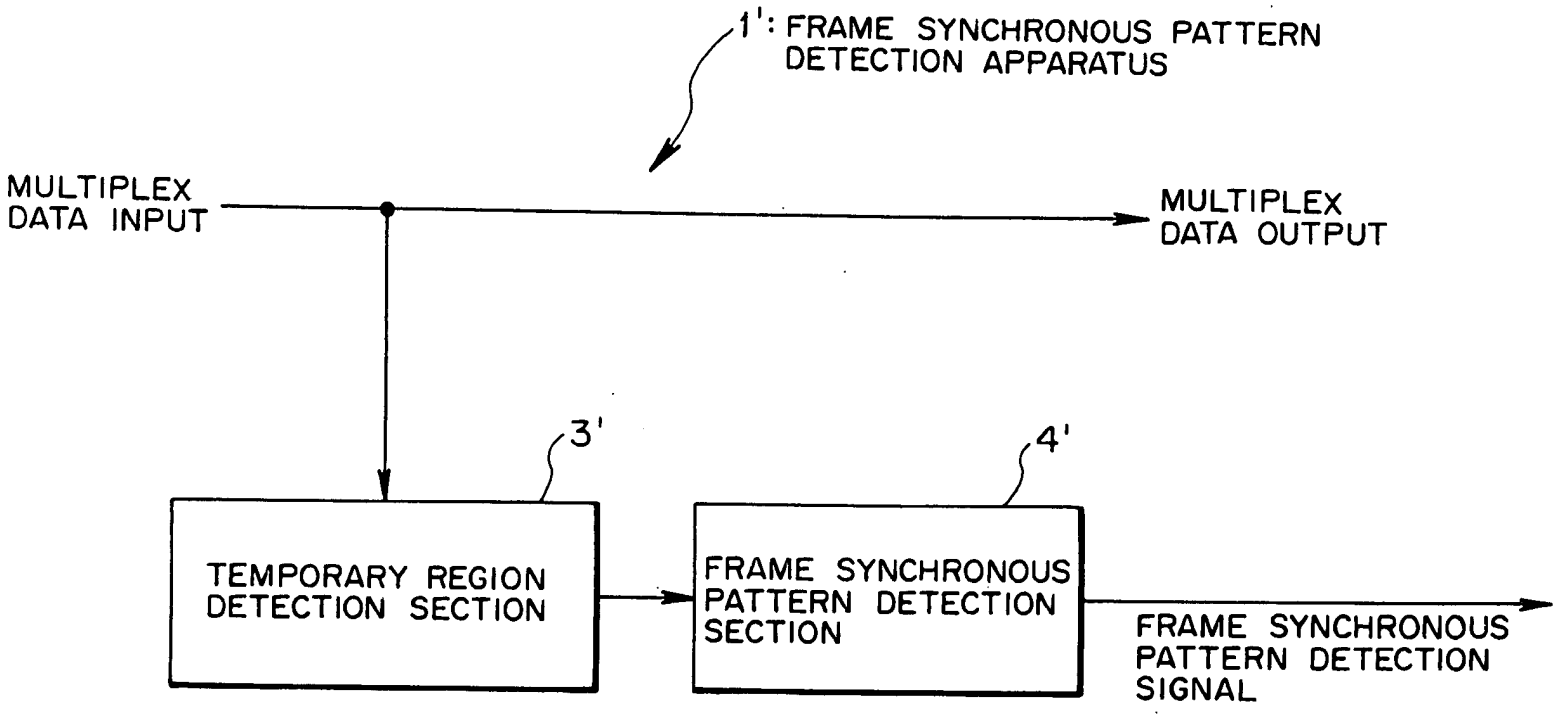

1': FRAME SYNCHRONOUS PATTERN DETECTION APPARATUS
MULTIPLEX DATA INPUT
MULTIPLEX DATA OUTPUT
3'
4'
TEMPORARY REGION DETECTION SECTION
FRAME SYNCHRONOUS PATTERN DETECTION SECTION
FRAME SYNCHRONOUS PATTERN DETECTION SIGNAL

FIG.3

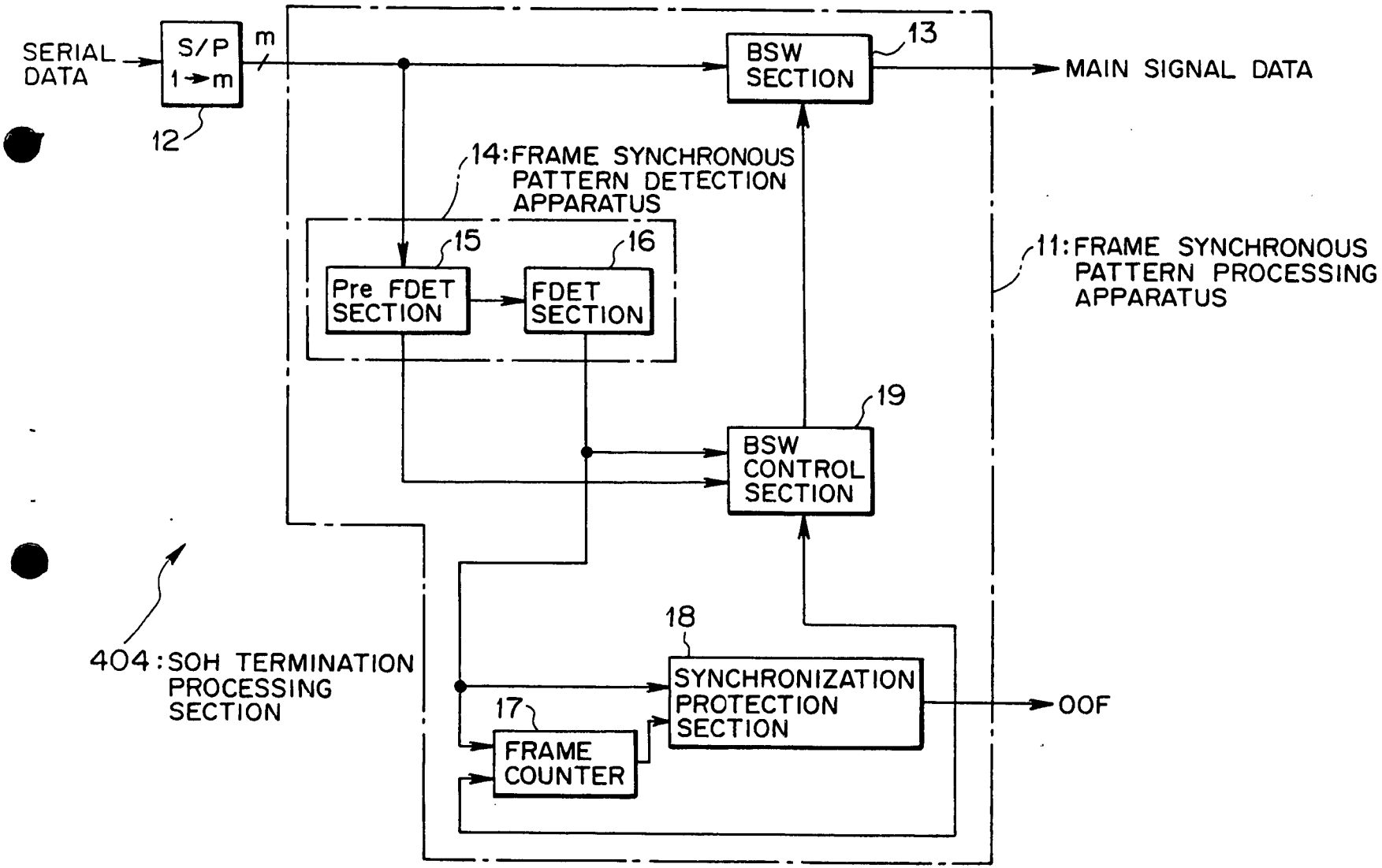

SERIAL DATA
S/P 1→m
m
12
BSW SECTION
13
MAIN SIGNAL DATA
14: FRAME SYNCHRONOUS PATTERN DETECTION APPARATUS
15
16
Pre FDET SECTION
FDET SECTION
11: FRAME SYNCHRONOUS PATTERN PROCESSING APPARATUS
19
BSW CONTROL SECTION
404: SOH TERMINATION PROCESSING SECTION
18
SYNCHRONIZATION PROTECTION SECTION
OOF
17
FRAME COUNTER

FIG.4

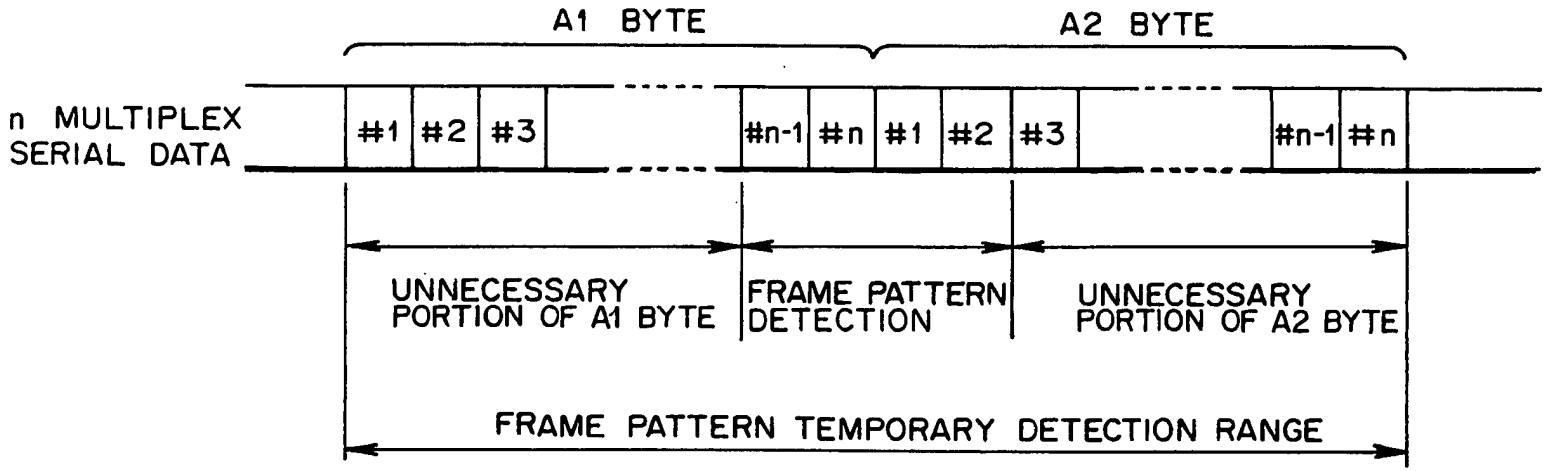

A1 BYTE
A2 BYTE
n MULTIPLEX SERIAL DATA
#1
#2
#3
#n-1
#n
#1
#2
#3
#n-1
#n
UNNECESSARY PORTION OF A1 BYTE
FRAME PATTERN DETECTION
UNNECESSARY PORTION OF A2 BYTE
FRAME PATTERN TEMPORARY DETECTION RANGE

FIG.5

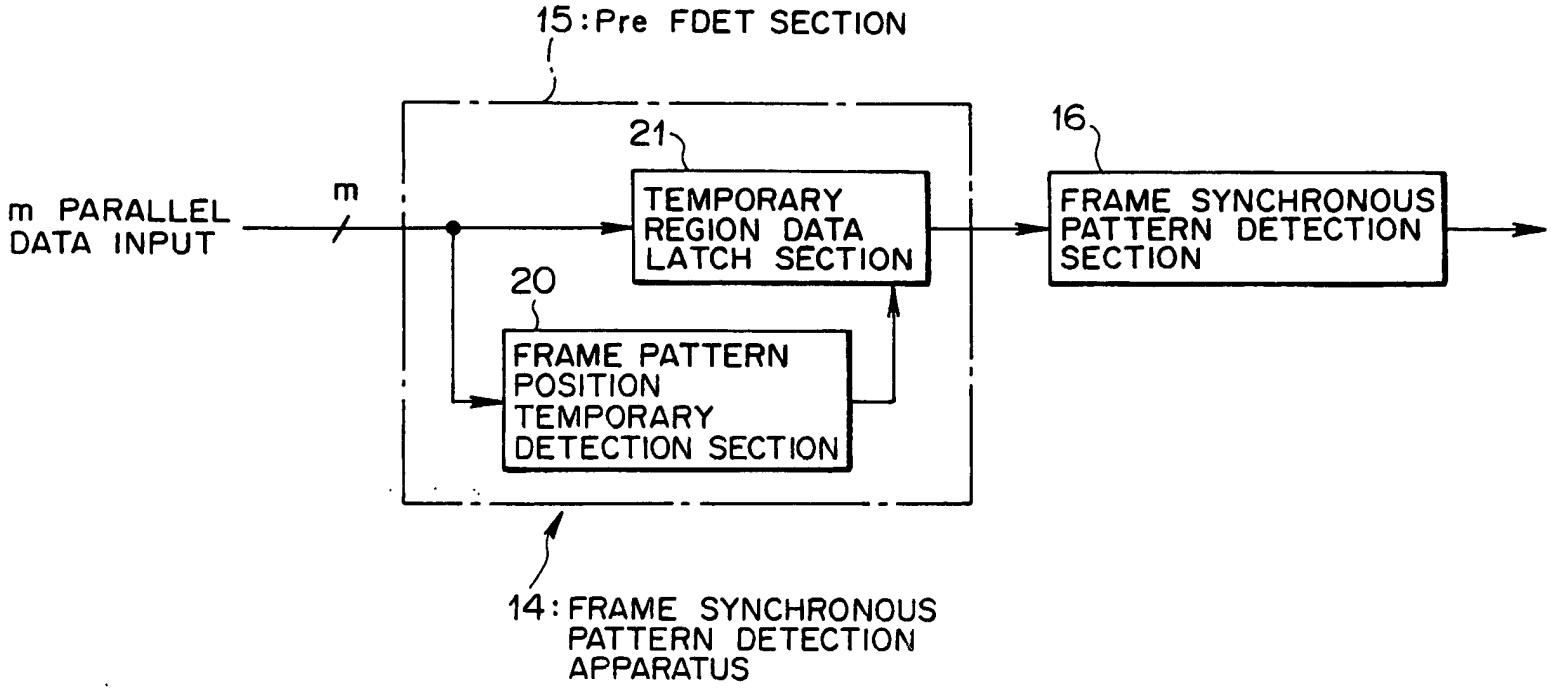

15 : Pre FDET SECTION
21
16
m PARALLEL DATA INPUT
m
TEMPORARY REGION DATA LATCH SECTION
FRAME SYNCHRONOUS PATTERN DETECTION SECTION
20
FRAME PATTERN POSITION TEMPORARY DETECTION SECTION
14 : FRAME SYNCHRONOUS PATTERN DETECTION APPARATUS

FIG.6

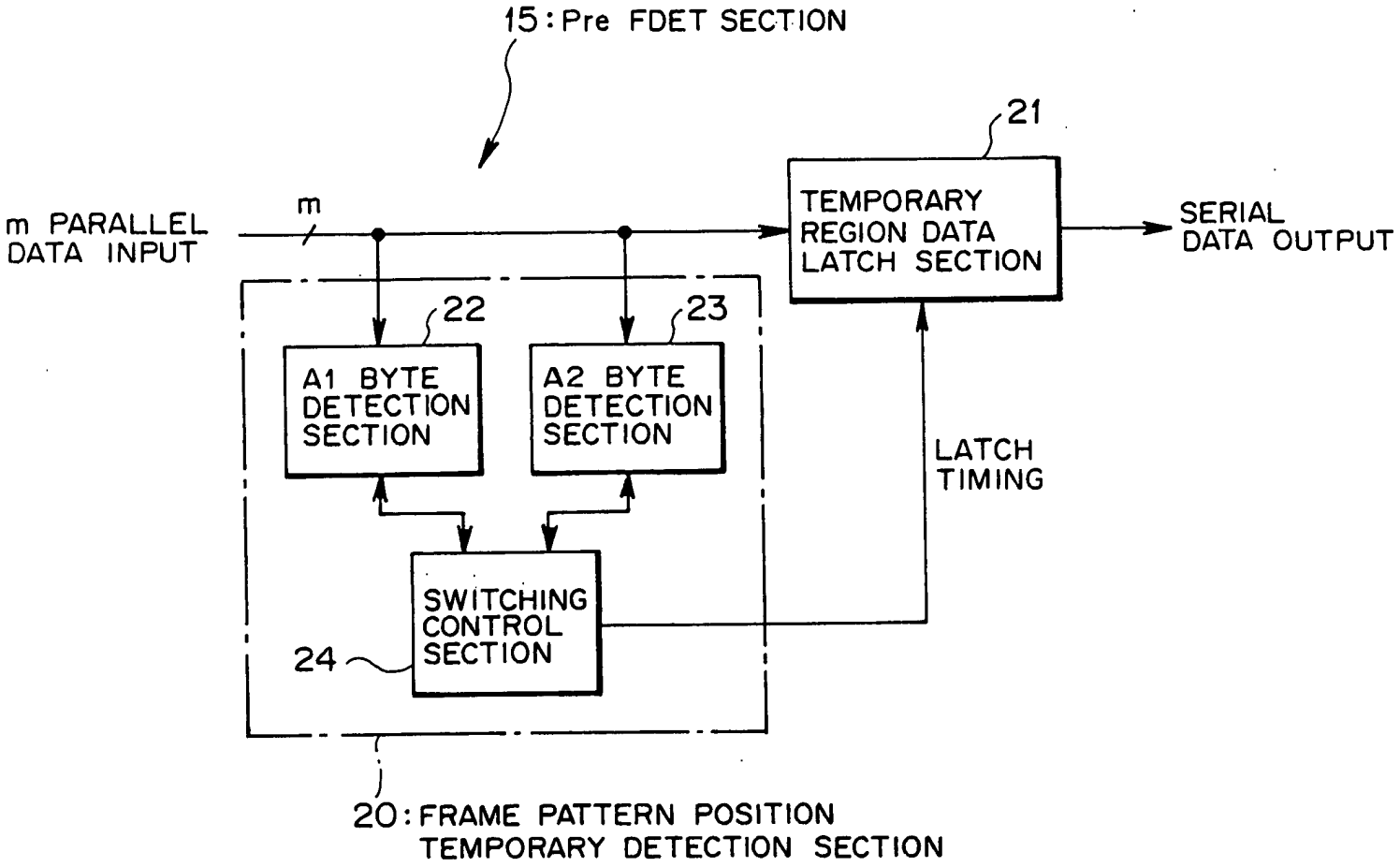

15 : Pre FDET SECTION
21
m PARALLEL DATA INPUT
m
TEMPORARY REGION DATA LATCH SECTION
SERIAL DATA OUTPUT
22
23
A1 BYTE DETECTION SECTION
A2 BYTE DETECTION SECTION
LATCH TIMING
SWITCHING CONTROL SECTION
24
20 : FRAME PATTERN POSITION TEMPORARY DETECTION SECTION

FIG. 7

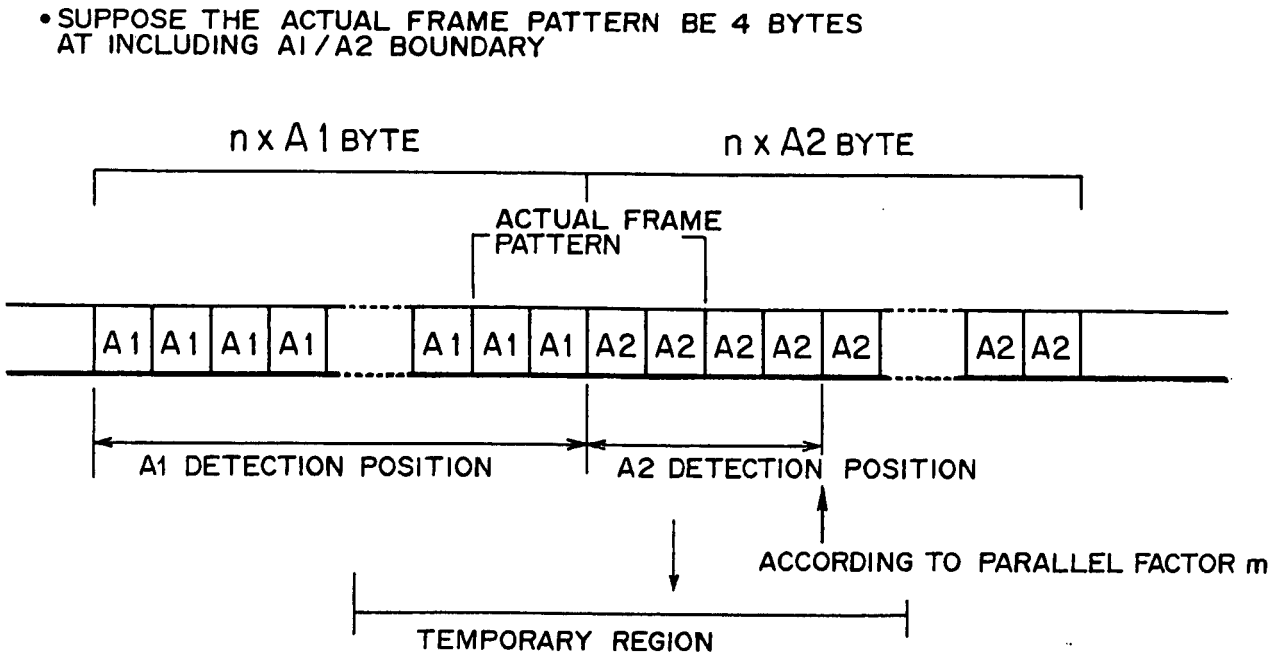
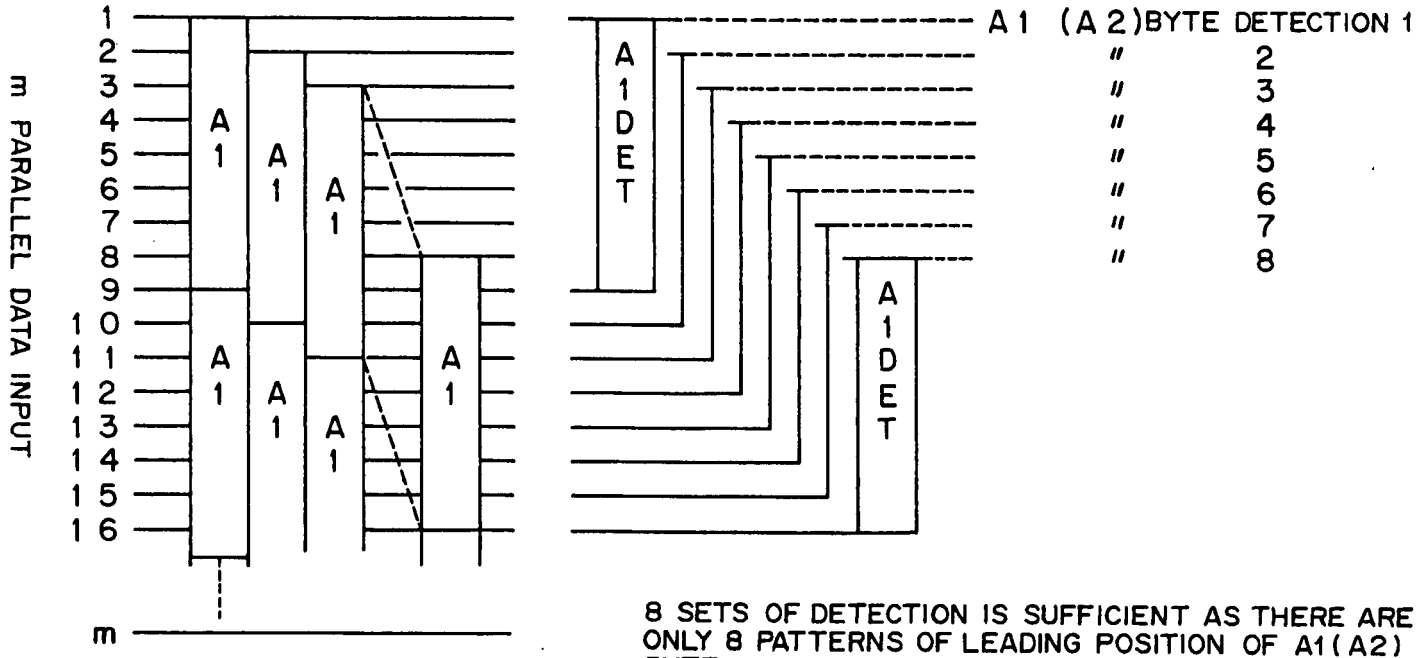

• SUPPOSE THE ACTUAL FRAME PATTERN BE 4 BYTES AT INCLUDING A1/A2 BOUNDARY
n x A1 BYTE
n x A2 BYTE
ACTUAL FRAME PATTERN
A1 A1 A1 A1 A1 A1 A1 A2 A2 A2 A2 A2 A2 A2
A1 DETECTION POSITION
A2 DETECTION POSITION
ACCORDING TO PARALLEL FACTOR m
TEMPORARY REGION

FIG. 8



8 SETS OF DETECTION IS SUFFICIENT AS THERE ARE ONLY 8 PATTERNS OF LEADING POSITION OF A1(A2) BYTE IN m PARALLEL DATA

FIG. 9

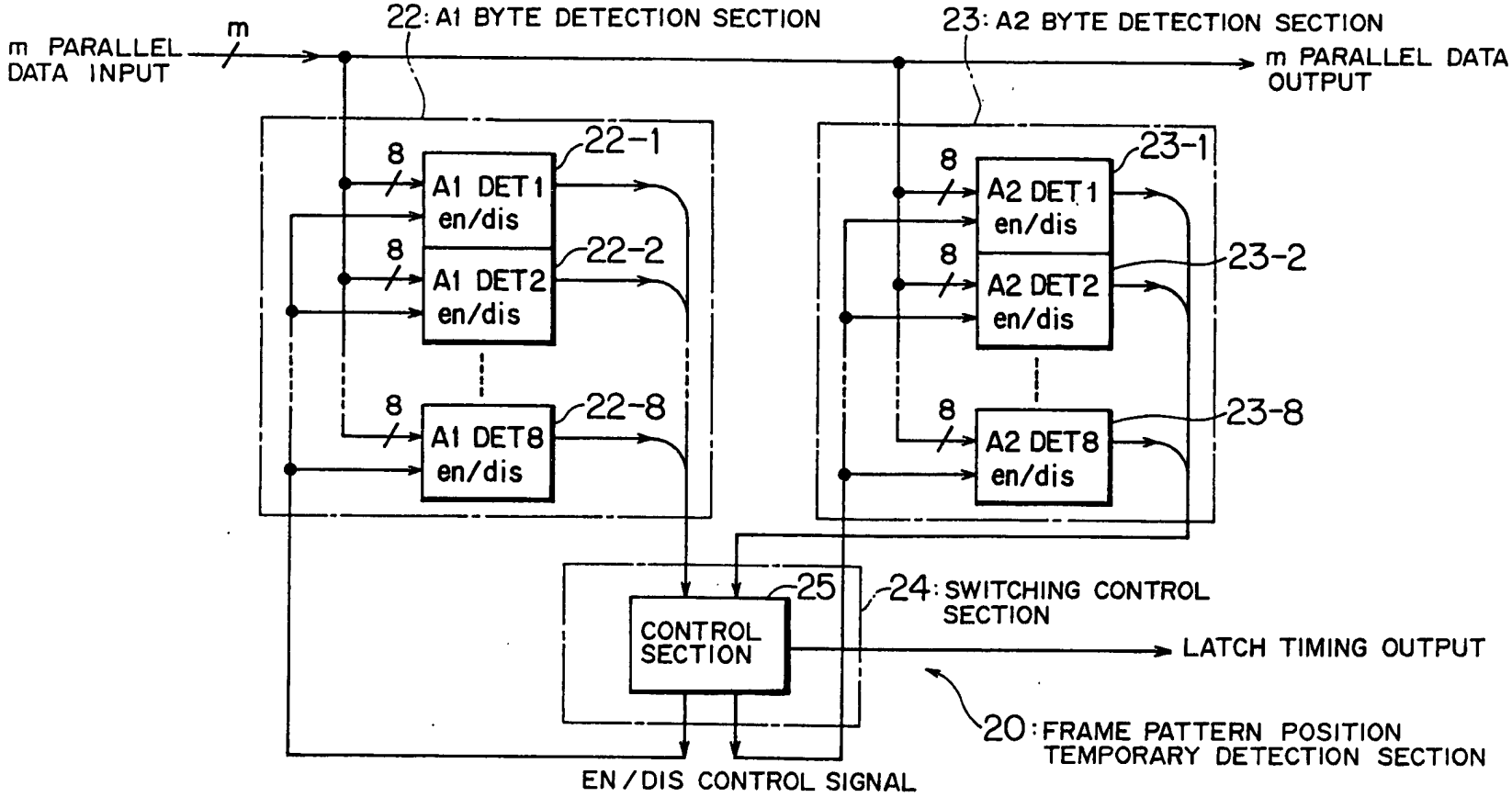

m PARALLEL DATA INPUT
m
22: A1 BYTE DETECTION SECTION
23: A2 BYTE DETECTION SECTION
m PARALLEL DATA OUTPUT
22-1
A1 DET1 en/dis
22-2
A1 DET2 en/dis
22-8
A1 DET8 en/dis
23-1
A2 DET1 en/dis
23-2
A2 DET2 en/dis
23-8
A2 DET8 en/dis
8
25
CONTROL SECTION
24: SWITCHING CONTROL SECTION
LATCH TIMING OUTPUT
20: FRAME PATTERN POSITION TEMPORARY DETECTION SECTION
EN/DIS CONTROL SIGNAL

FIG. 10

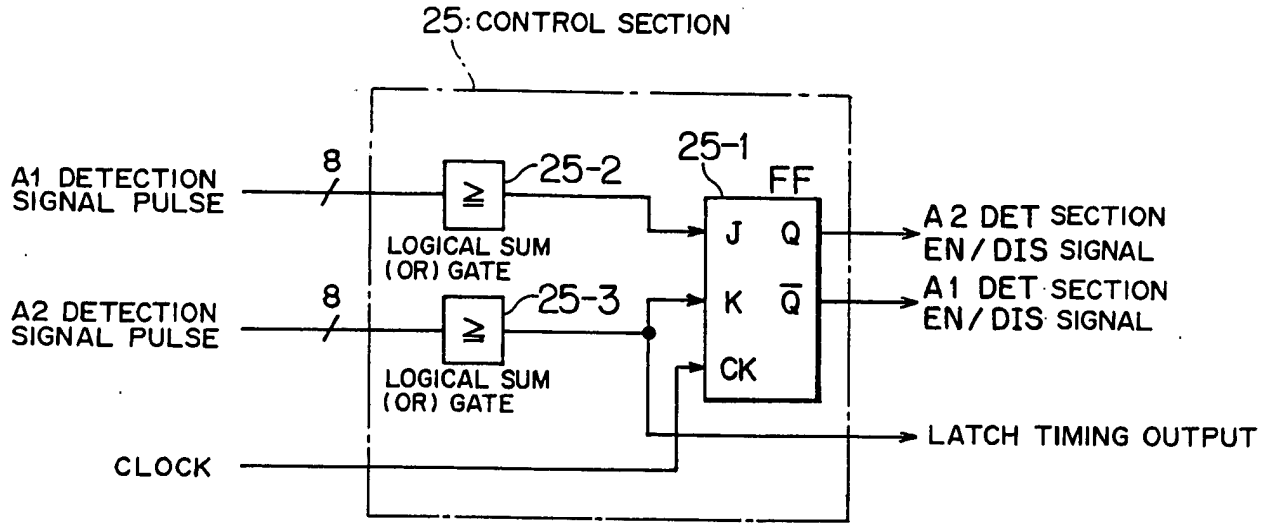
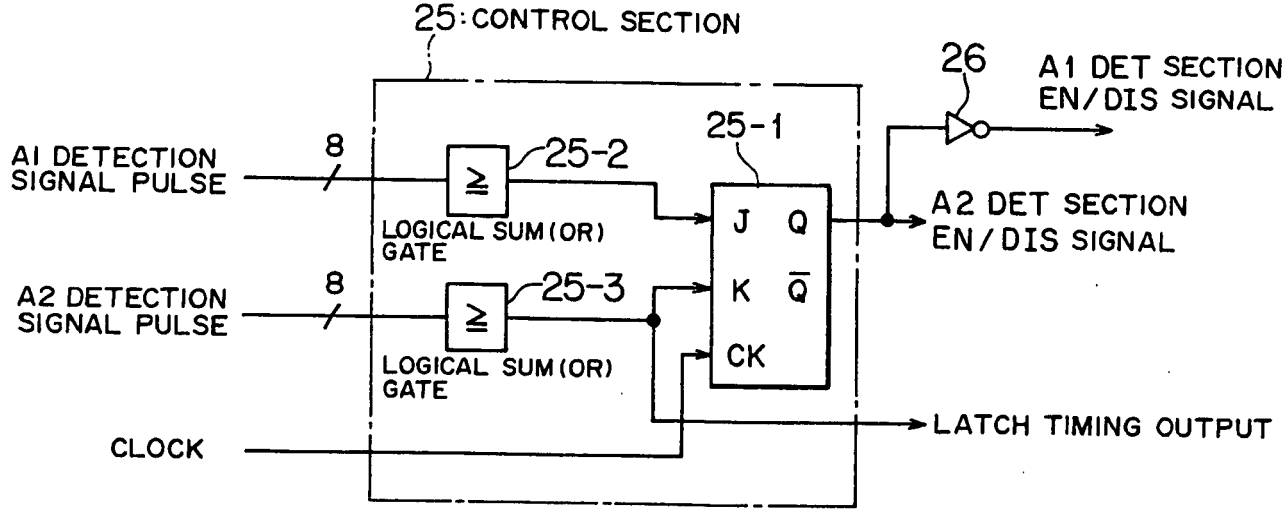

25: CONTROL SECTION
A1 DETECTION SIGNAL PULSE
8
25-2
25-1
FF
LOGICAL SUM (OR) GATE
J
Q
A2 DET SECTION EN/DIS SIGNAL
A2 DETECTION SIGNAL PULSE
8
25-3
K
Q̄
A1 DET SECTION EN/DIS SIGNAL
LOGICAL SUM (OR) GATE
CK
LATCH TIMING OUTPUT
CLOCK

FIG. 11


25: CONTROL SECTION
26
A1 DET SECTION EN/DIS SIGNAL
25-1
A1 DETECTION SIGNAL PULSE
8
25-2
≧
LOGICAL SUM (OR) GATE
J
Q
A2 DET SECTION EN/DIS SIGNAL
A2 DETECTION SIGNAL PULSE
8
25-3
≧
LOGICAL SUM (OR) GATE
K
$\bar{Q}$
CK
CLOCK
LATCH TIMING OUTPUT

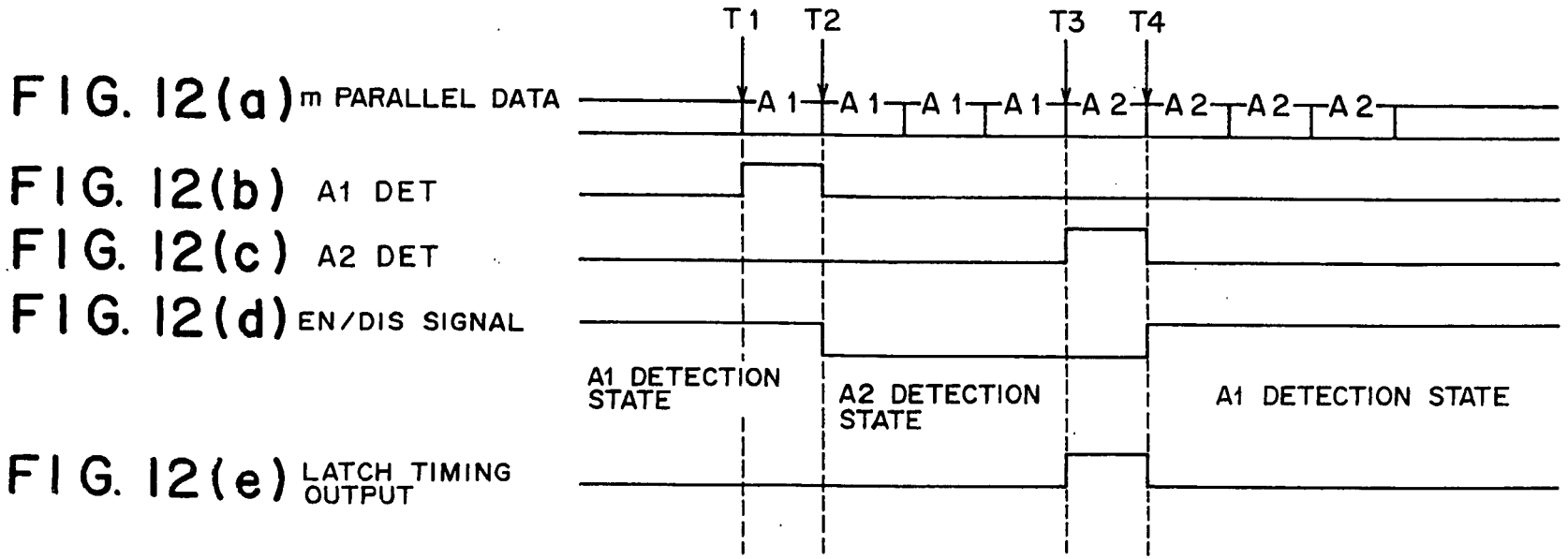


FIG. 12(a) m PARALLEL DATA

FIG. 12(b) A1 DET

FIG. 12(c) A2 DET

FIG. 12(d) EN/DIS SIGNAL

FIG. 12(e) LATCH TIMING OUTPUT

FIG. 13(a) CLOCK

FIG. 13(b) A1 DETECTION SIGNAL PULSE

FIG. 13(c) A2 DETECTION SIGNAL PULSE

FIG. 13(d) A2 DET SECTION EN/DIS SIGNAL

FIG. 13(e) LATCH TIMING OUTPUT

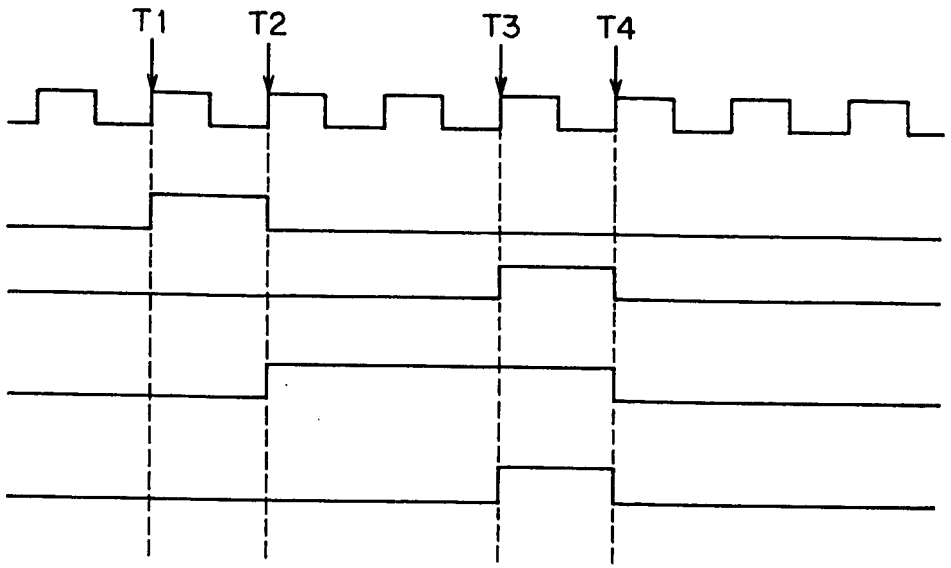


FIG. 14

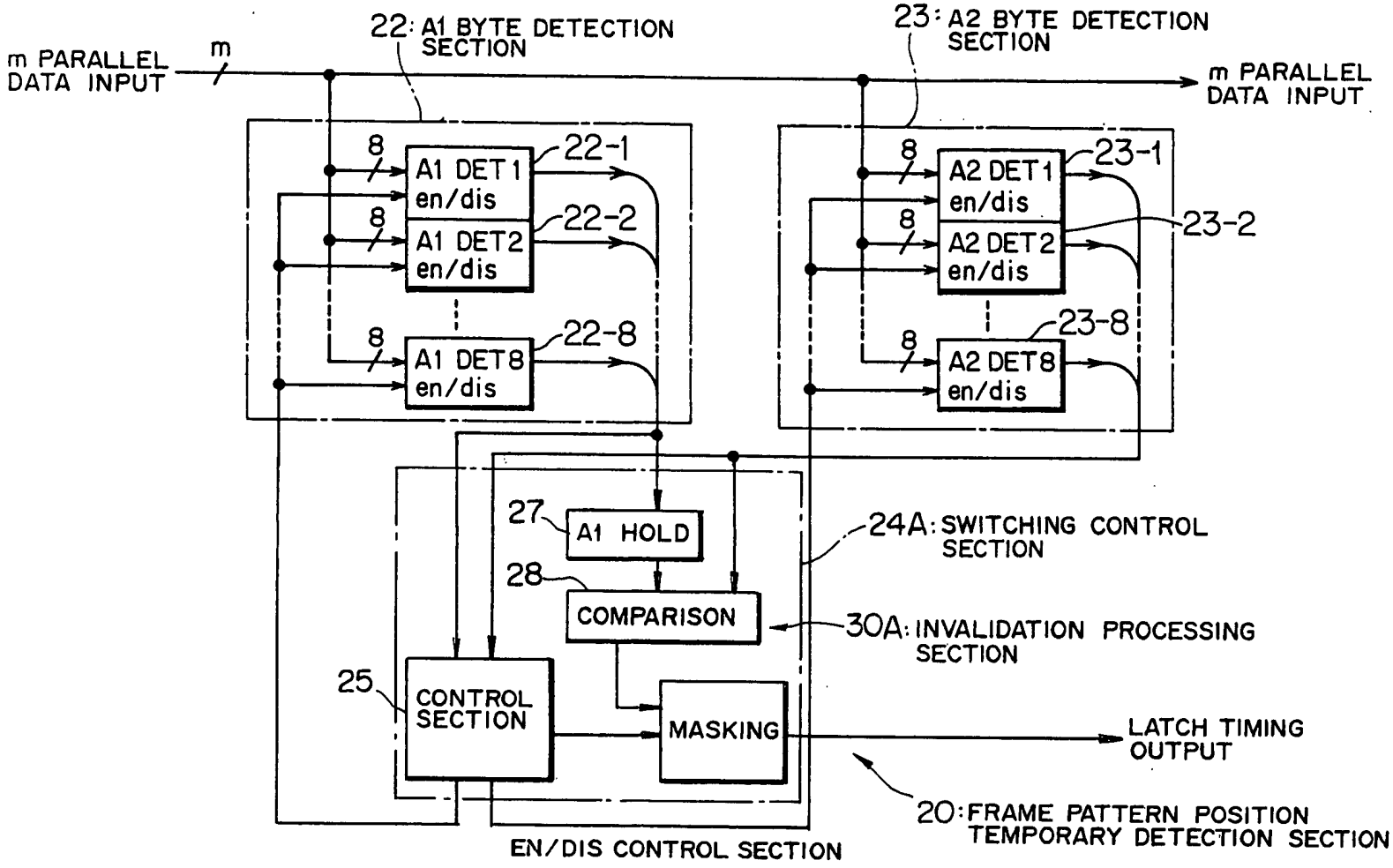
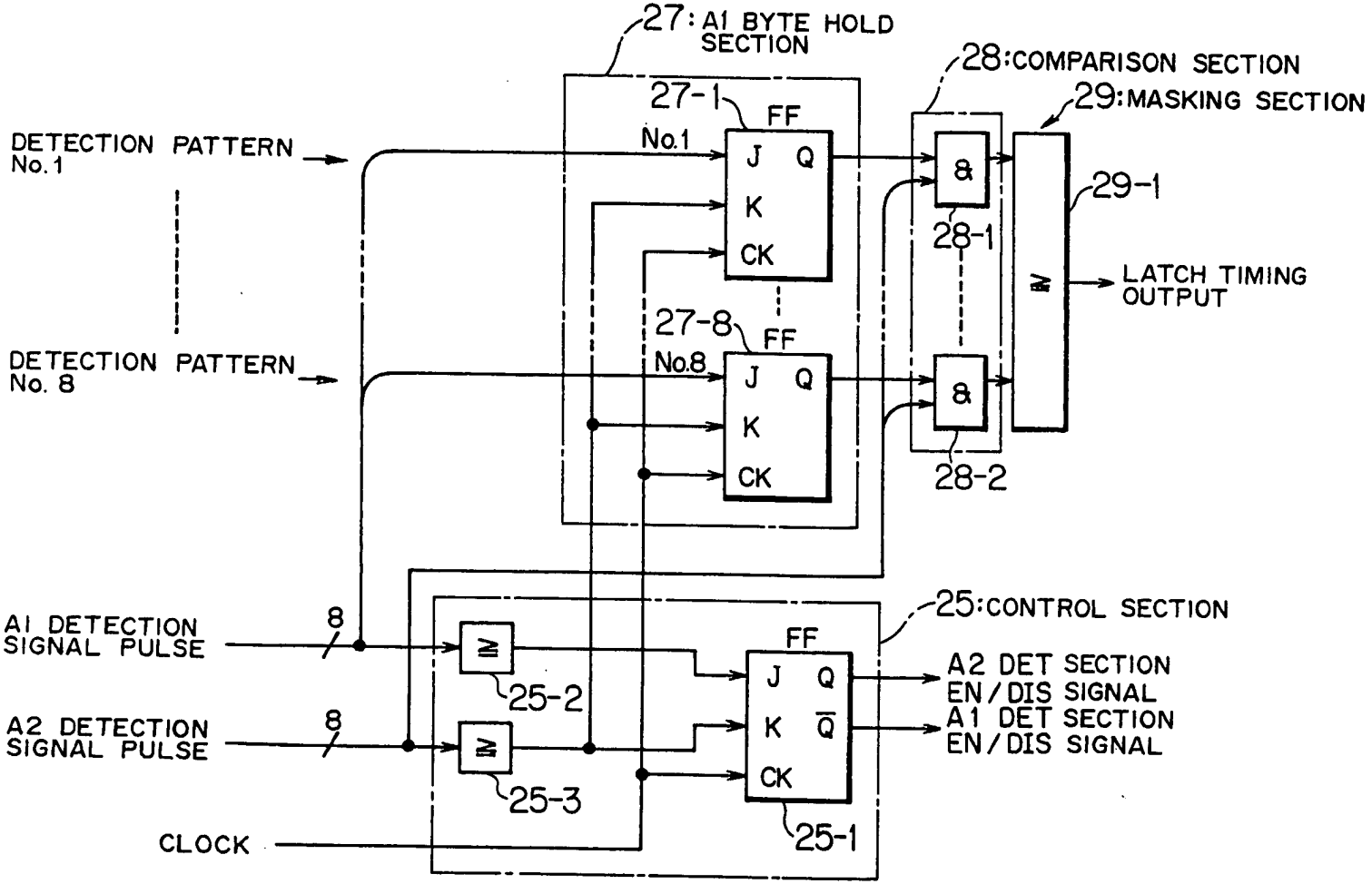

m PARALLEL DATA INPUT
m
22: A1 BYTE DETECTION SECTION
23: A2 BYTE DETECTION SECTION
m PARALLEL DATA INPUT
8
A1 DET1 en/dis
22-1
A1 DET2 en/dis
22-2
A1 DET8 en/dis
22-8
A2 DET1 en/dis
23-1
A2 DET2 en/dis
23-2
A2 DET8 en/dis
23-8
27
A1 HOLD
28
COMPARISON
24A: SWITCHING CONTROL SECTION
30A: INVALIDATION PROCESSING SECTION
25
CONTROL SECTION
MASKING
LATCH TIMING OUTPUT
20: FRAME PATTERN POSITION TEMPORARY DETECTION SECTION
EN/DIS CONTROL SECTION

FIG. 15


27: A1 BYTE HOLD SECTION
28: COMPARISON SECTION
29: MASKING SECTION
27-1
FF
No.1
J Q
K
CK
27-8
No.8
DETECTION PATTERN No. 1
DETECTION PATTERN No. 8
&
28-1
28-2
29-1
LATCH TIMING OUTPUT
A1 DETECTION SIGNAL PULSE
A2 DETECTION SIGNAL PULSE
8
≧
25-2
25-3
25: CONTROL SECTION
FF
J Q
K Q̄
CK
25-1
A2 DET SECTION EN/DIS SIGNAL
A1 DET SECTION EN/DIS SIGNAL
CLOCK

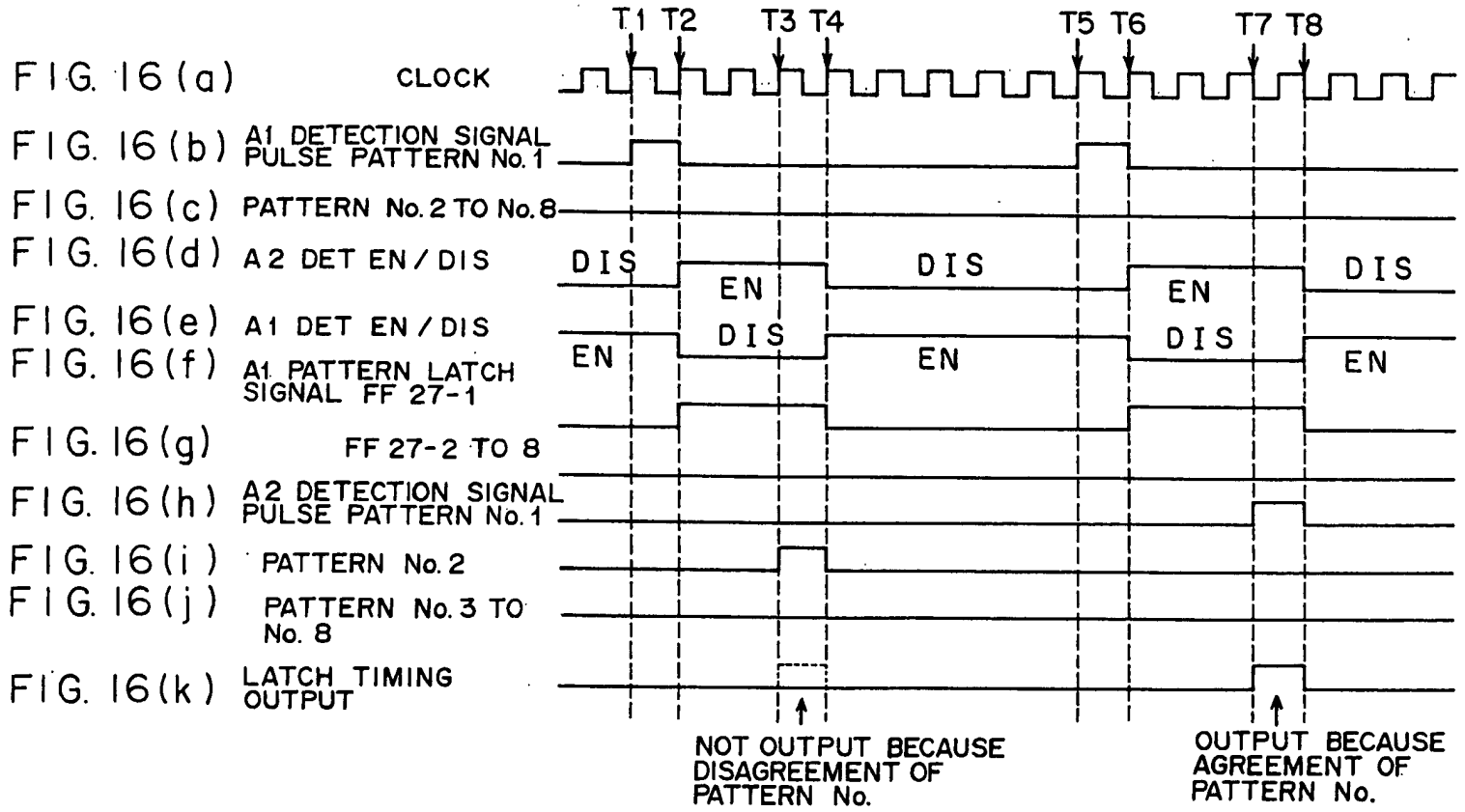

T1 T2
T3 T4
T5 T6
T7 T8
FIG. 16(a) CLOCK
FIG. 16(b) A1 DETECTION SIGNAL PULSE PATTERN No. 1
FIG. 16(c) PATTERN No. 2 TO No. 8
FIG. 16(d) A2 DET EN / DIS
DIS
EN
DIS
DIS
EN
DIS
FIG. 16(e) A1 DET EN / DIS
EN
DIS
EN
EN
FIG. 16(f) A1 PATTERN LATCH SIGNAL FF 27-1
FIG. 16(g) FF 27-2 TO 8
FIG. 16(h) A2 DETECTION SIGNAL PULSE PATTERN No. 1
FIG. 16(i) PATTERN No. 2
FIG. 16(j) PATTERN No. 3 TO No. 8
FIG. 16(k) LATCH TIMING OUTPUT
NOT OUTPUT BECAUSE DISAGREEMENT OF PATTERN No.
OUTPUT BECAUSE AGREEMENT OF PATTERN No.

FIG. 17

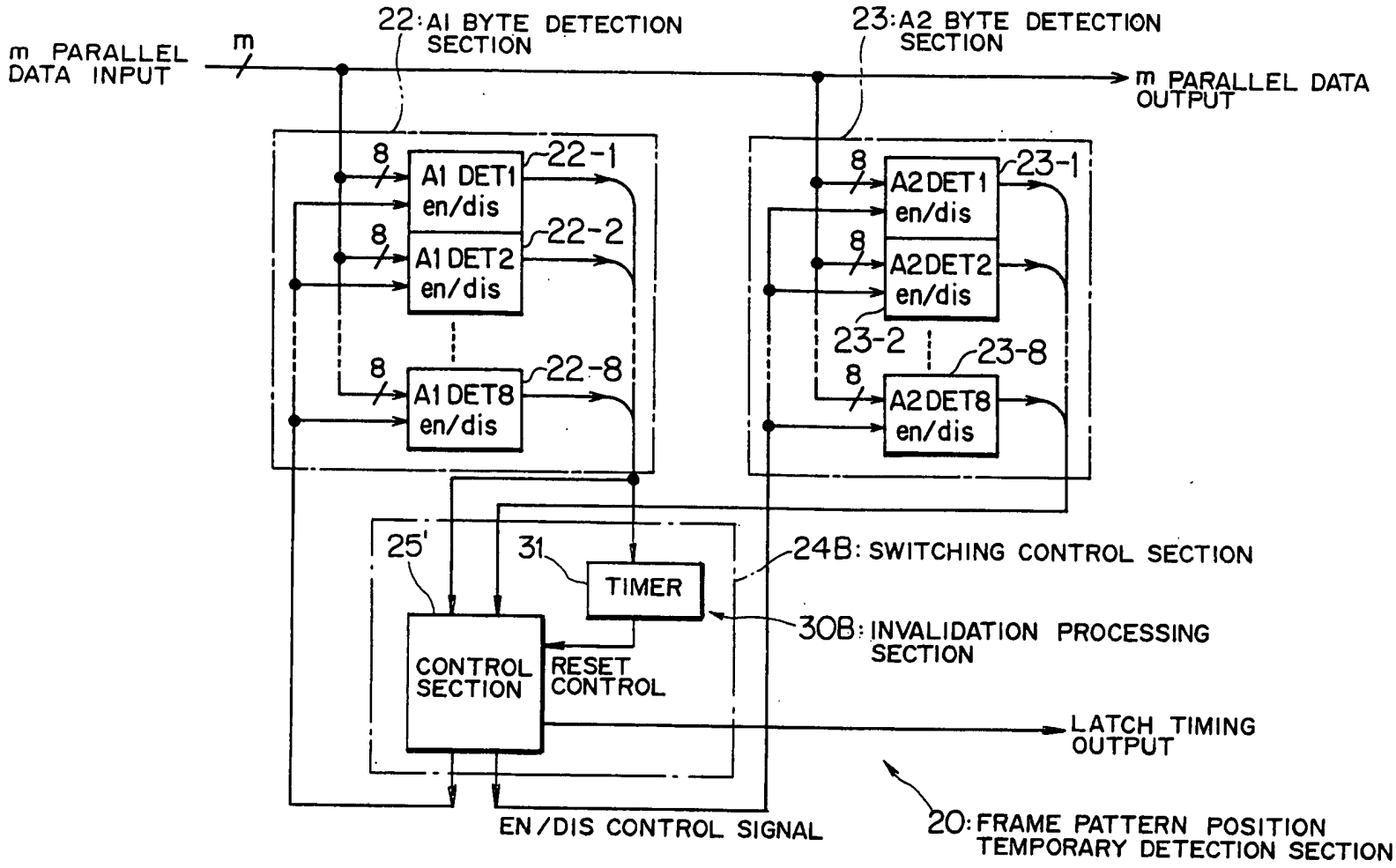

m PARALLEL DATA INPUT
m
22: A1 BYTE DETECTION SECTION
23: A2 BYTE DETECTION SECTION
m PARALLEL DATA OUTPUT
8
A1 DET1 en/dis
22-1
A1 DET2 en/dis
22-2
A1 DET8 en/dis
22-8
A2DET1 en/dis
23-1
A2DET2 en/dis
23-2
A2DET8 en/dis
23-8
25'
31
TIMER
24B: SWITCHING CONTROL SECTION
30B: INVALIDATION PROCESSING SECTION
CONTROL SECTION
RESET CONTROL
LATCH TIMING OUTPUT
EN/DIS CONTROL SIGNAL
20: FRAME PATTERN POSITION TEMPORARY DETECTION SECTION

FIG. 18

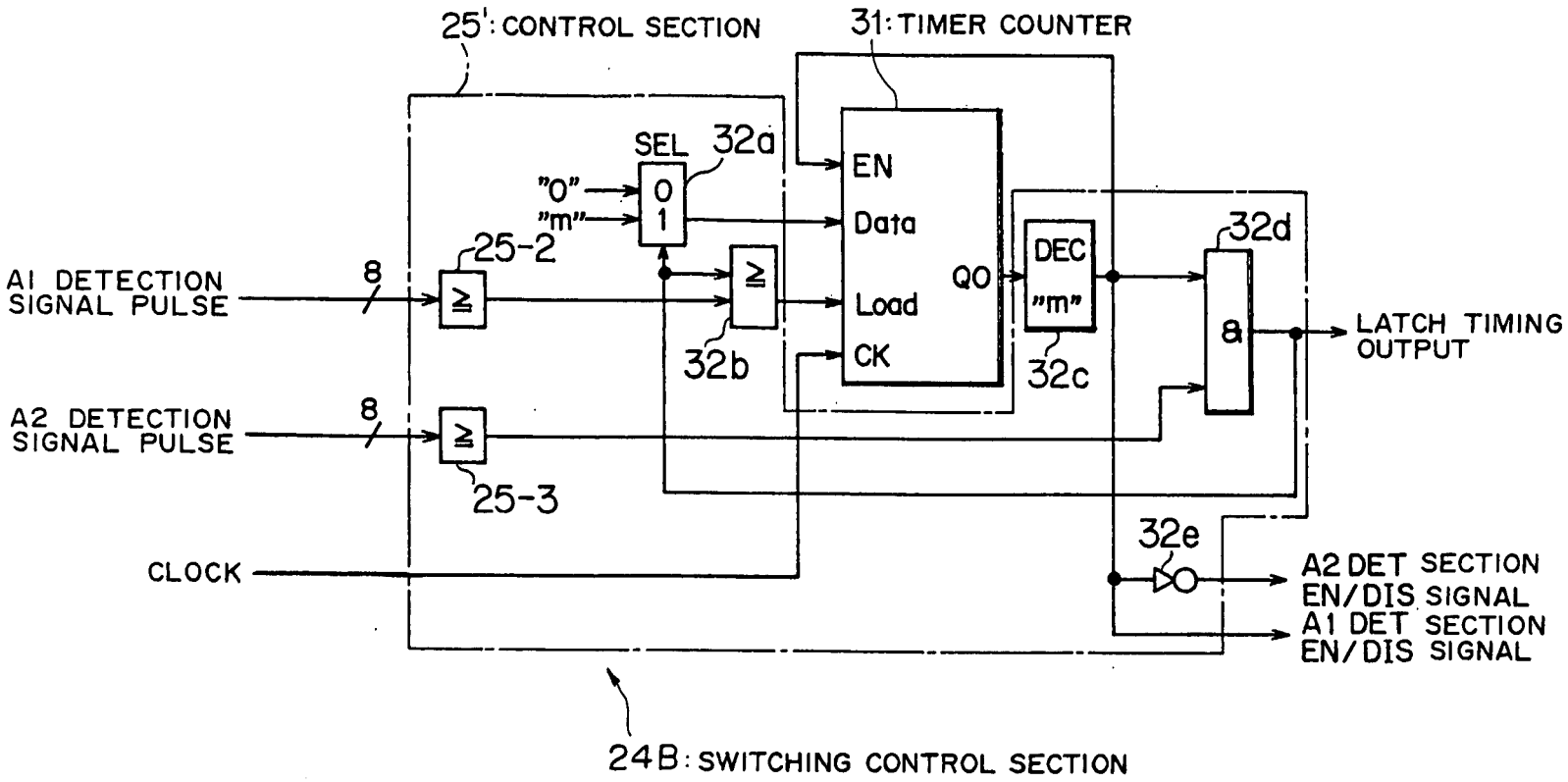

25': CONTROL SECTION
31: TIMER COUNTER
SEL
32a
"0"
"m"
0
1
EN
Data
Load
CK
Q0
DEC
"m"
32c
32d
8a
LATCH TIMING OUTPUT
A1 DETECTION SIGNAL PULSE
8
25-2
≧
32b
A2 DETECTION SIGNAL PULSE
8
25-3
CLOCK
32e
A2 DET SECTION EN/DIS SIGNAL
A1 DET SECTION EN/DIS SIGNAL
24B: SWITCHING CONTROL SECTION

FIG. 19(a) LOAD INPUT

FIG. 19(b) Q OUTPUT

FIG. 19(c) A2 INPUT

FIG. 19(d) LATCH TIMING

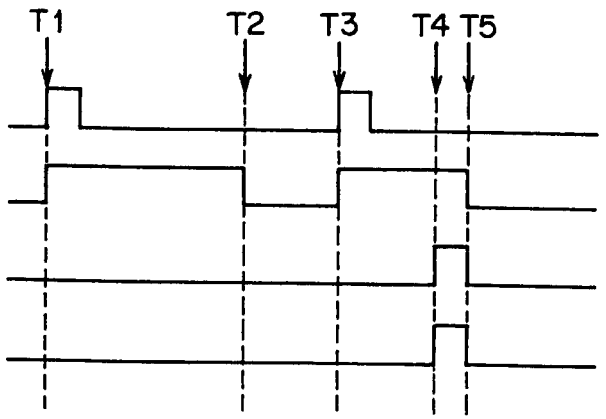


FIG. 20(a) m PARALLEL DATA

FIG. 20(b) A1 DET

FIG. 20(c) A2 DET

FIG. 20(d) TIMER OUTPUT

FIG. 20(e) EN/DIS CONTROL SIGNAL

FIG. 20(f) LATCH TIMING OUTPUT

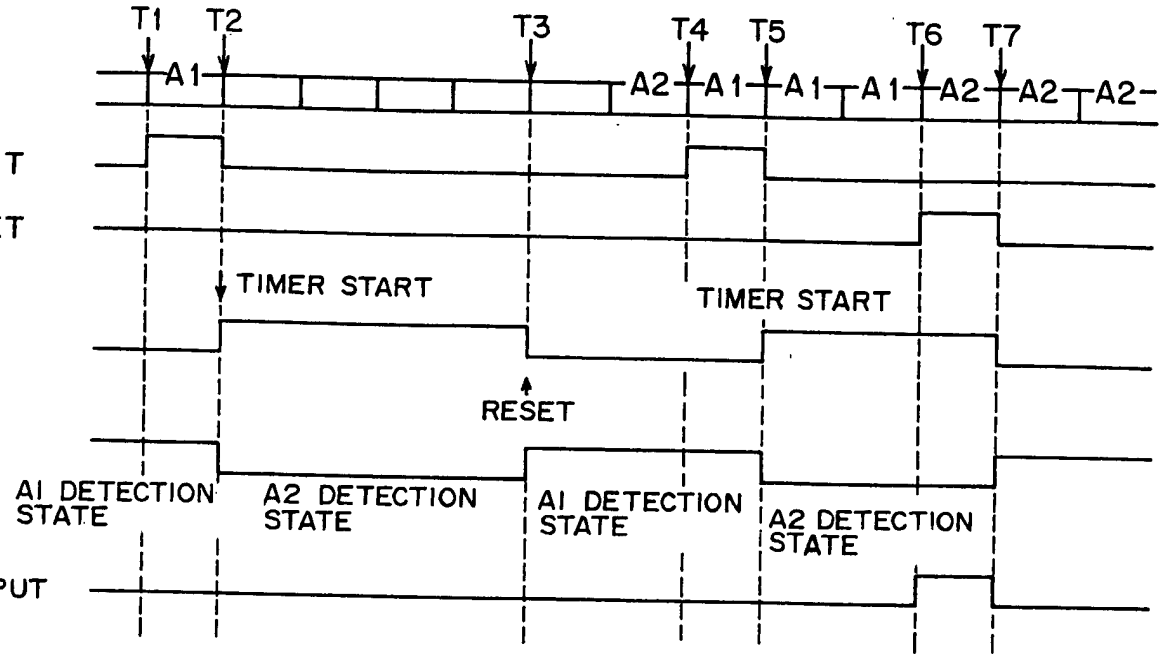


FIG. 21

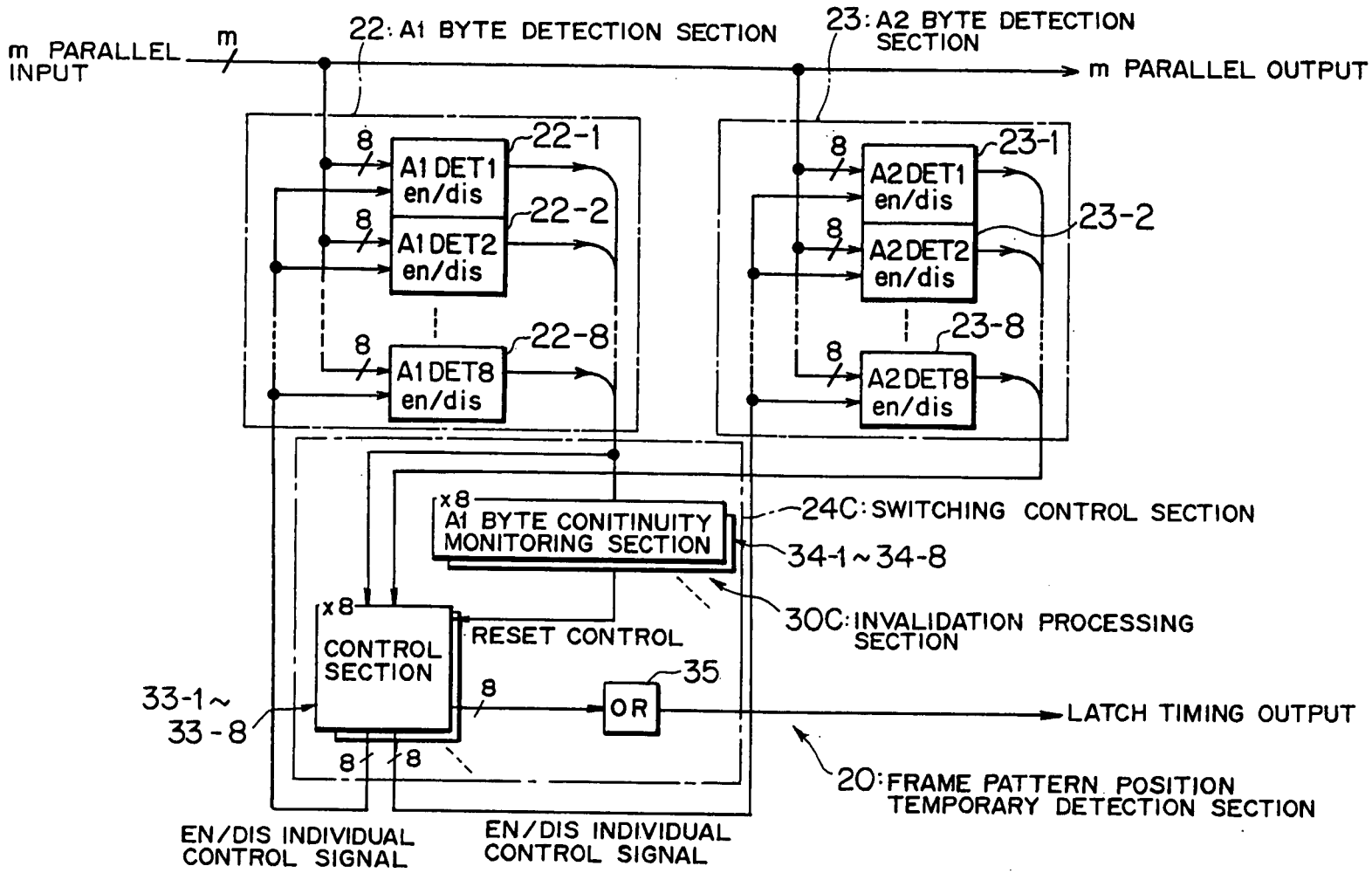

m PARALLEL INPUT
m
22: A1 BYTE DETECTION SECTION
23: A2 BYTE DETECTION SECTION
m PARALLEL OUTPUT
8
A1 DET1 en/dis
22-1
A1 DET2 en/dis
22-2
A1 DET8 en/dis
22-8
A2 DET1 en/dis
23-1
A2 DET2 en/dis
23-2
A2 DET8 en/dis
23-8
x8
A1 BYTE CONITINUITY MONITORING SECTION
24C: SWITCHING CONTROL SECTION
34-1 ~ 34-8
30C: INVALIDATION PROCESSING SECTION
CONTROL SECTION
RESET CONTROL
33-1 ~ 33-8
OR
35
LATCH TIMING OUTPUT
20: FRAME PATTERN POSITION TEMPORARY DETECTION SECTION
EN/DIS INDIVIDUAL CONTROL SIGNAL
EN/DIS INDIVIDUAL CONTROL SIGNAL

FIG. 22

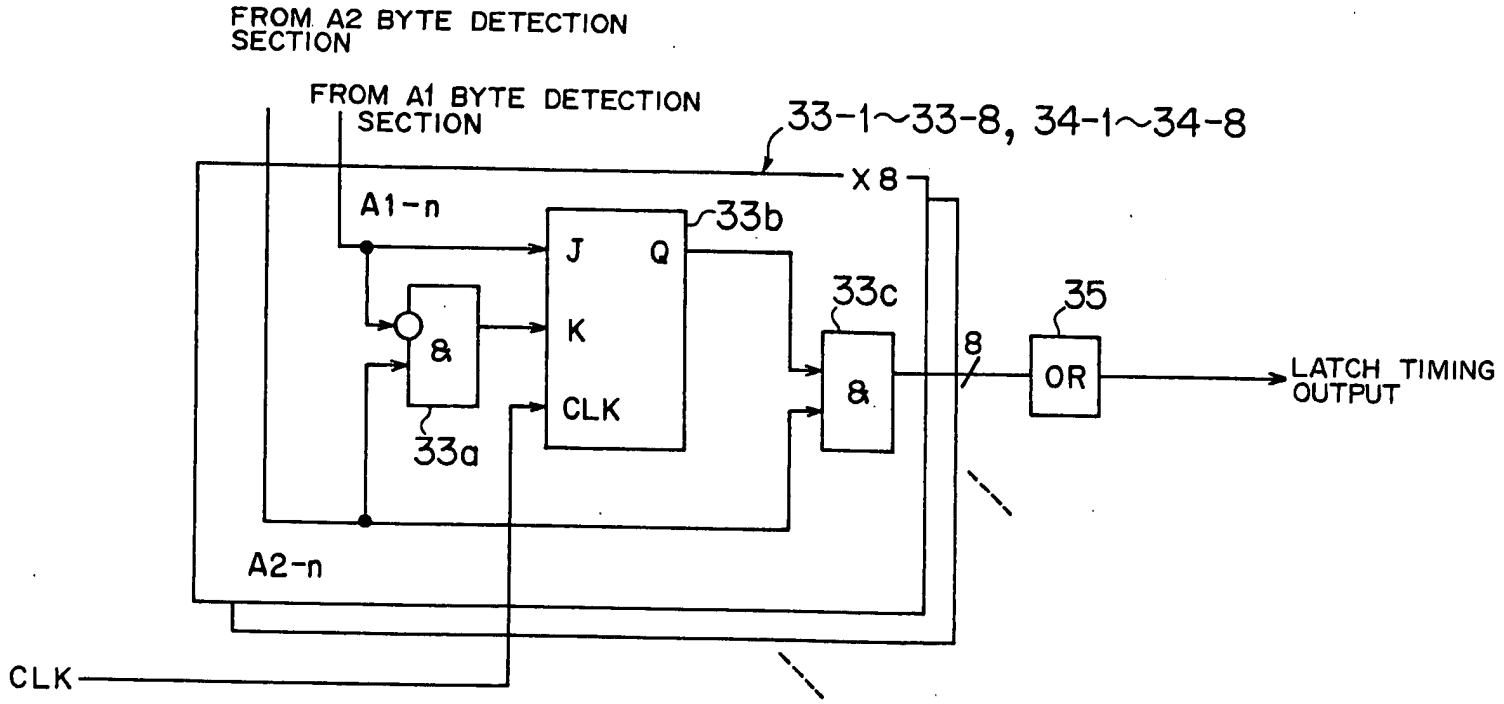

FROM A2 BYTE DETECTION SECTION
FROM A1 BYTE DETECTION SECTION
33-1~33-8, 34-1~34-8
X 8
A1-n
33b
J
Q
K
CLK
&
33a
33c
&
8
35
OR
LATCH TIMING OUTPUT
A2-n
CLK

FIG. 23(a) m PARALLEL DATA

FIG. 23(b) A1 DET

FIG. 23(c) A2 DET

FIG. 23(d) EN/DIS CONTROL

FIG. 23(e) LATCH TIMING OUTPUT

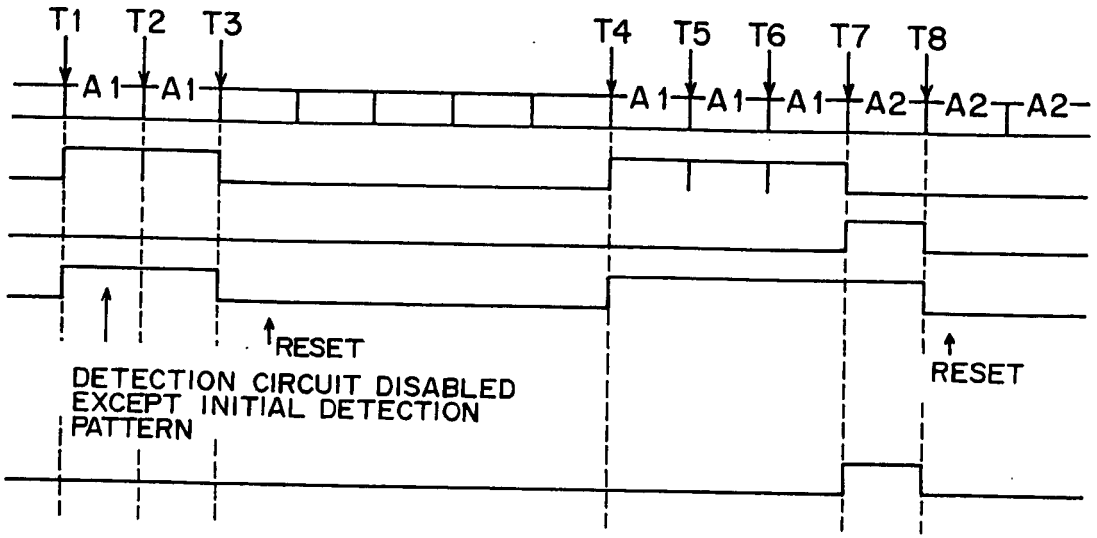


FIG. 24

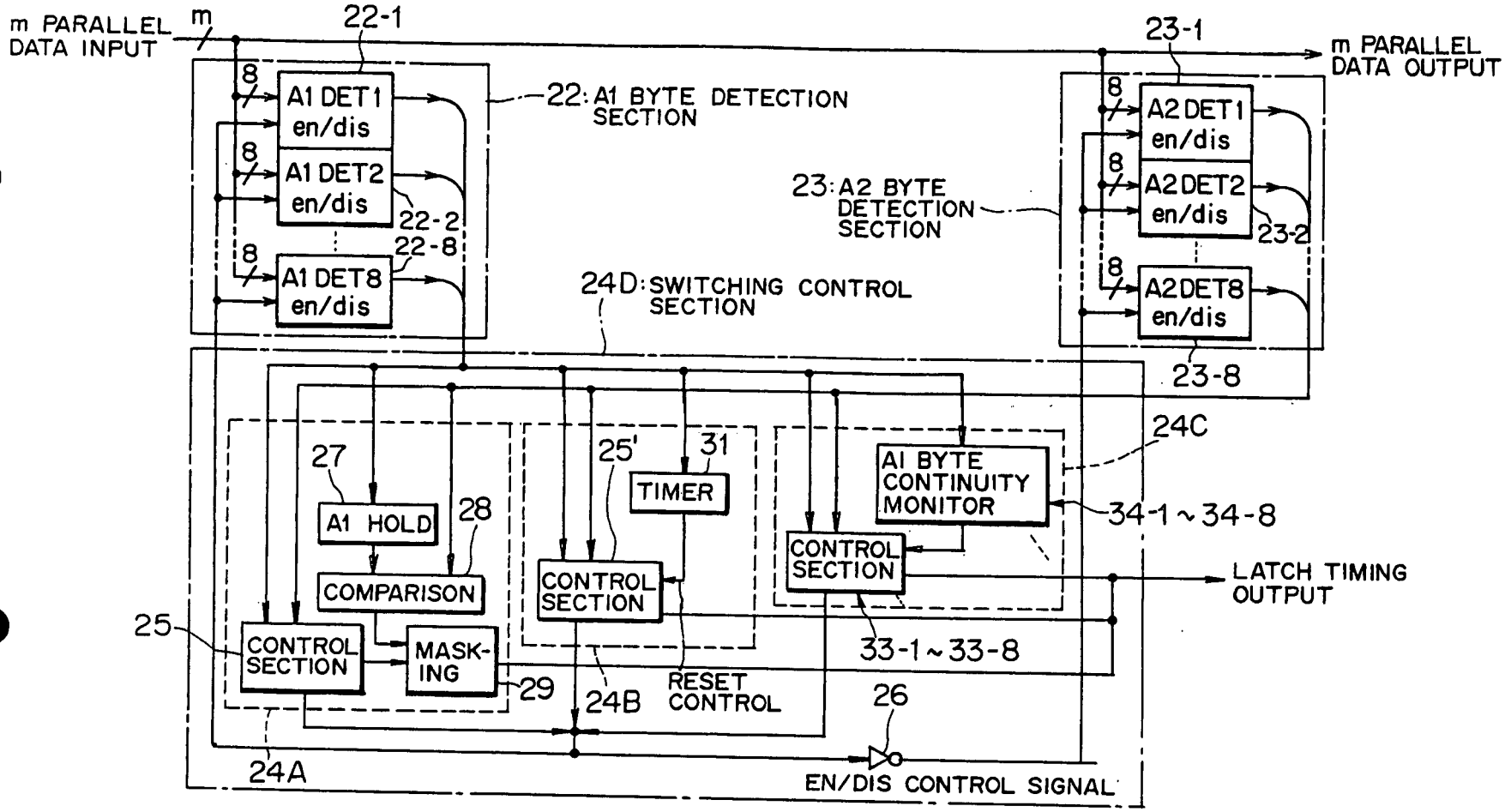

m PARALLEL DATA INPUT
m
22-1
23-1
m PARALLEL DATA OUTPUT
8
A1 DET1 en/dis
A1 DET2 en/dis
A1 DET8 en/dis
22-2
22-8
22: A1 BYTE DETECTION SECTION
23: A2 BYTE DETECTION SECTION
A2 DET1 en/dis
A2 DET2 en/dis
A2 DET8 en/dis
23-2
23-8
24D: SWITCHING CONTROL SECTION
24C
27
A1 HOLD
28
COMPARISON
25
CONTROL SECTION
MASK-ING
29
25'
31
TIMER
CONTROL SECTION
24B
RESET CONTROL
A1 BYTE CONTINUITY MONITOR
34-1 ~ 34-8
CONTROL SECTION
LATCH TIMING OUTPUT
33-1 ~ 33-8
26
24A
EN/DIS CONTROL SIGNAL

FIG.25

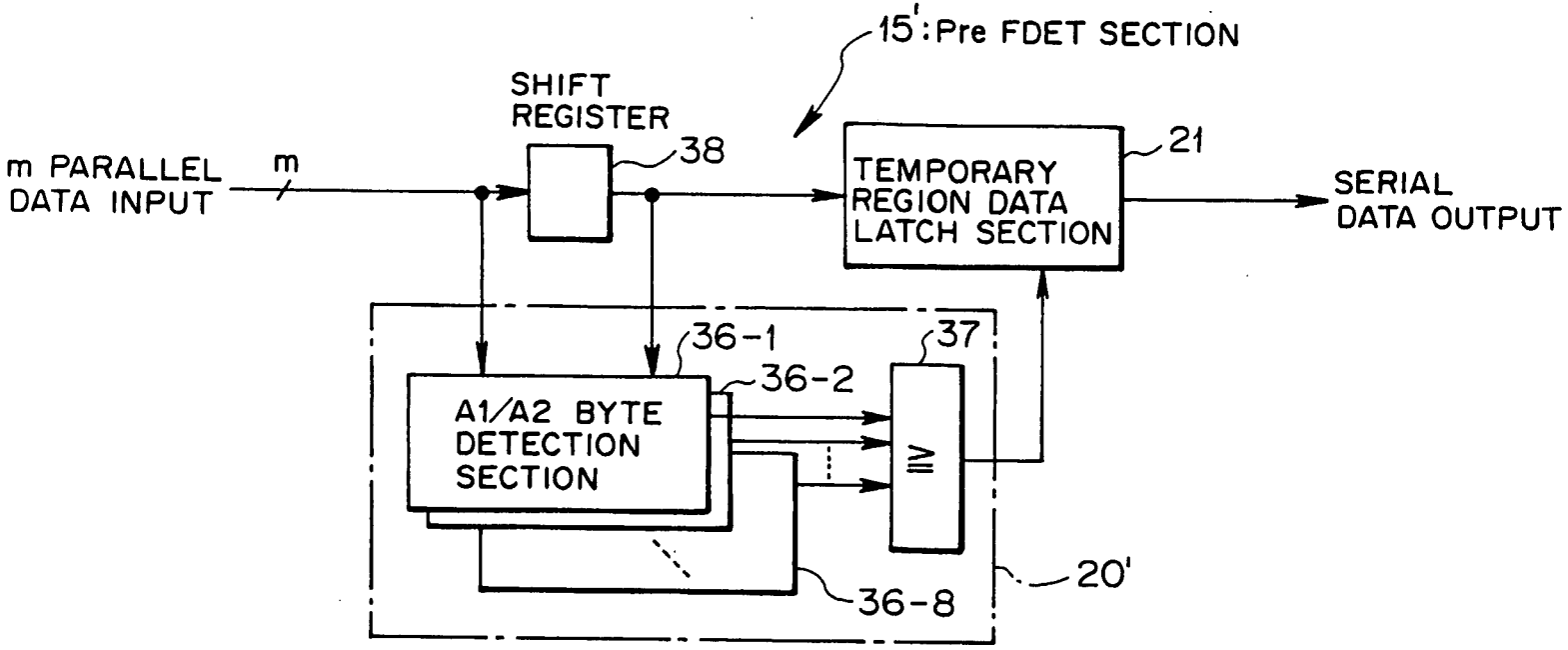

15': Pre FDET SECTION
SHIFT REGISTER
38
m PARALLEL DATA INPUT
m
TEMPORARY REGION DATA LATCH SECTION
21
SERIAL DATA OUTPUT
36-1
36-2
37
A1/A2 BYTE DETECTION SECTION
≧
20'
36-8

FIG.26

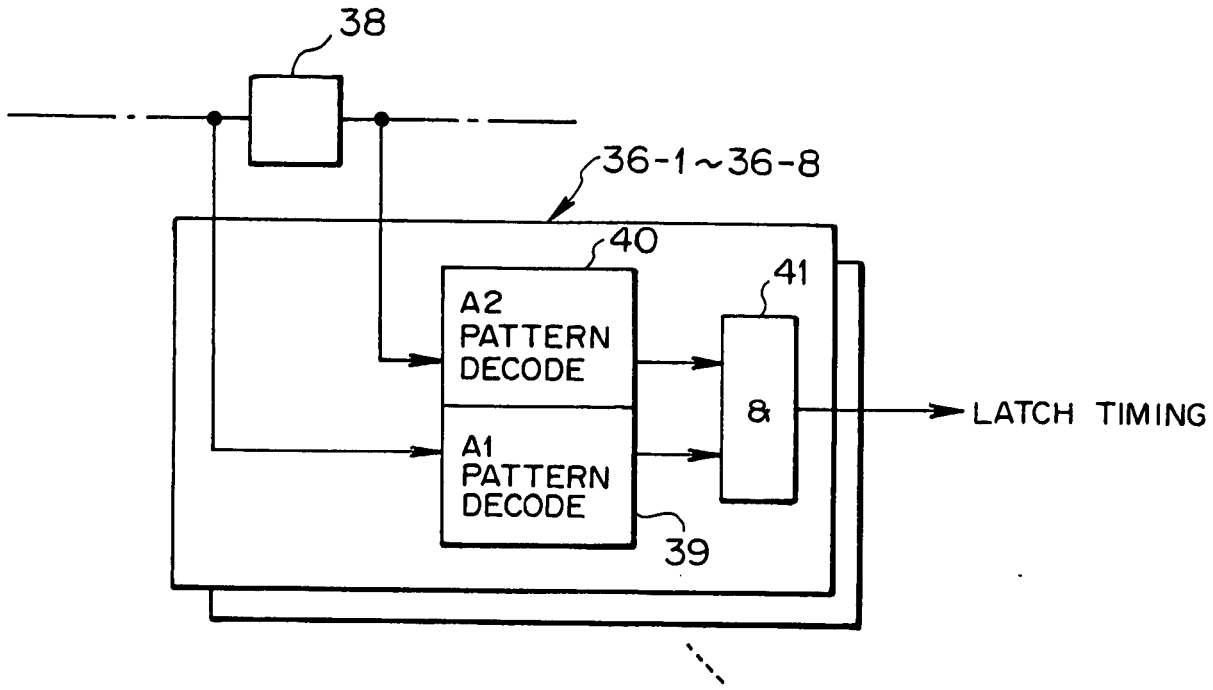

38
36-1~36-8
40
41
A2
PATTERN
DECODE
A1
PATTERN
DECODE
&
LATCH TIMING
39

FIG. 27(a)

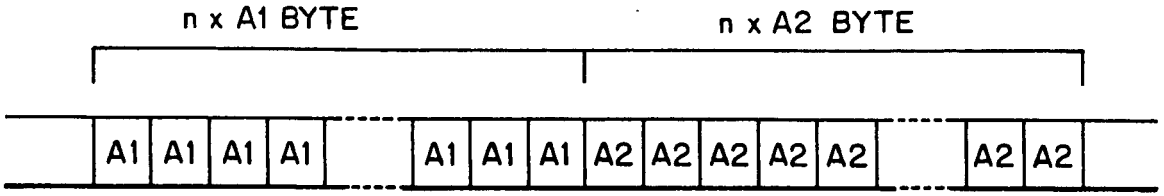


FIG. 27(b)

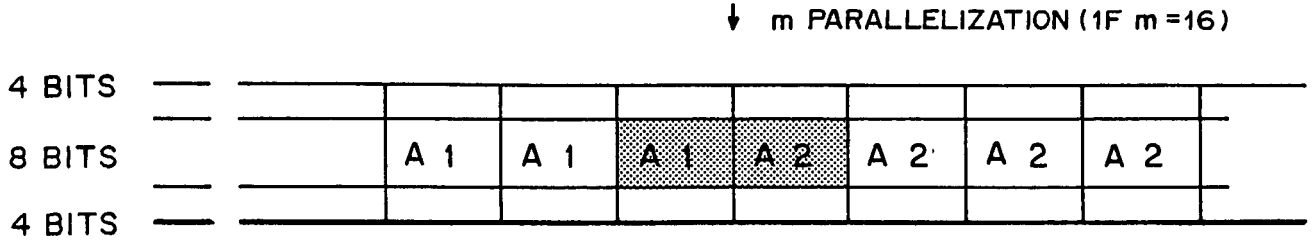
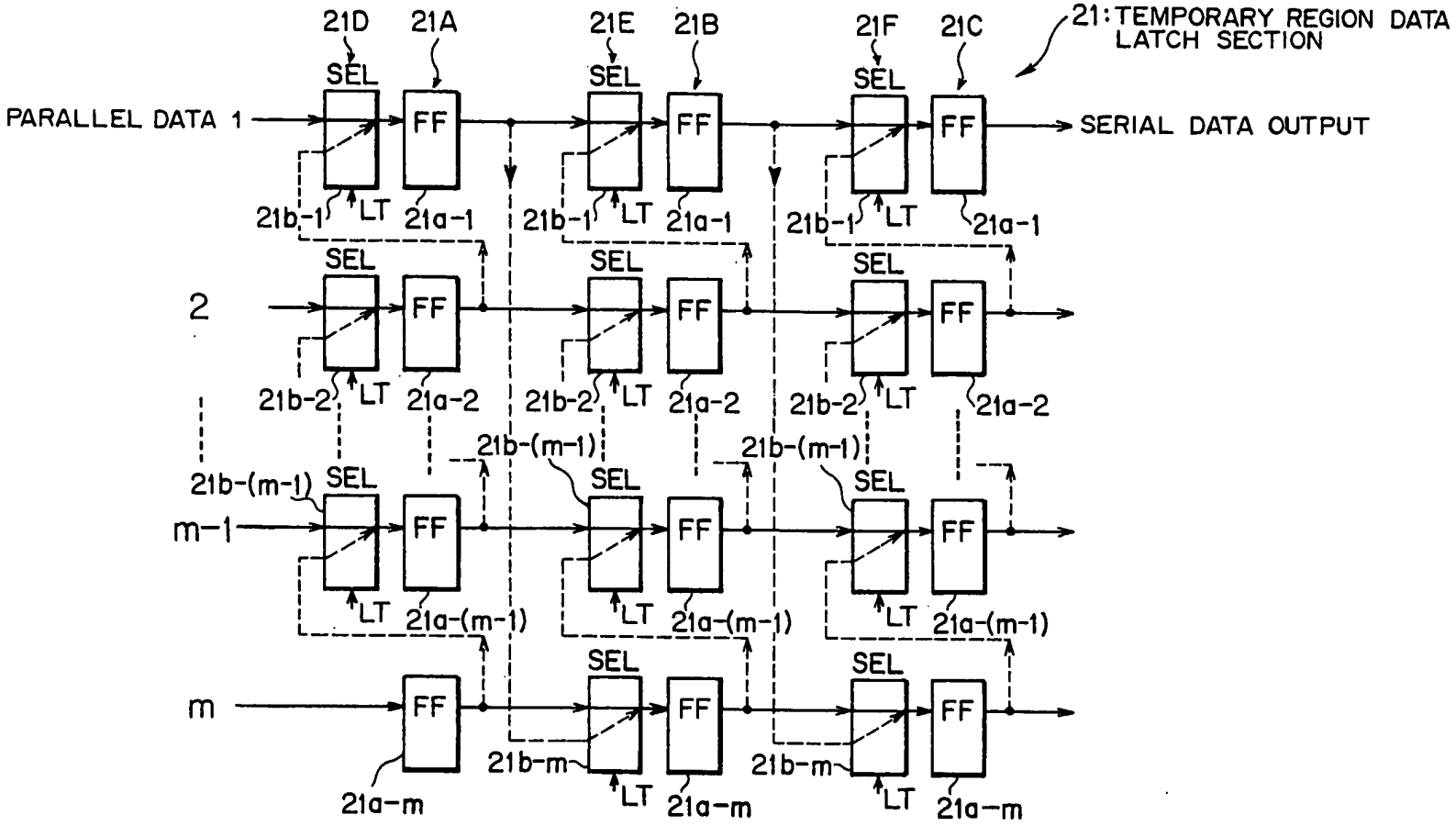


FIG. 28



LT: LATCH TIMING SIGNAL

FIG. 29

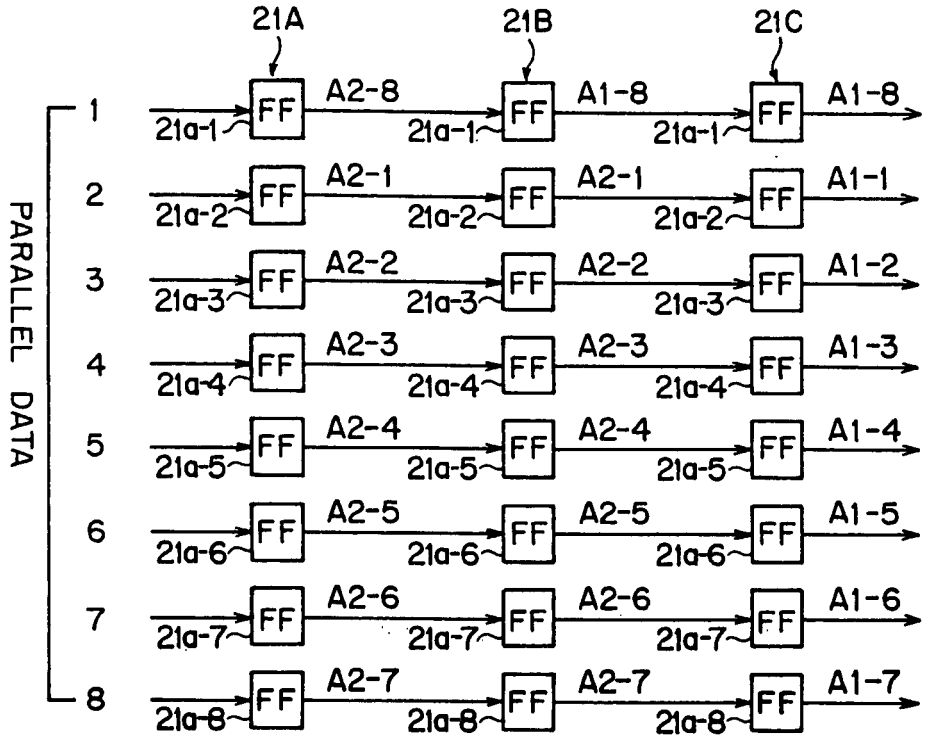

21A
21B
21C
PARALLEL DATA
1
2
3
4
5
6
7
8
FF
A2-8
A1-8
A1-8
A2-1
A2-1
A1-1
A2-2
A2-2
A1-2
A2-3
A2-3
A1-3
A2-4
A2-4
A1-4
A2-5
A2-5
A1-5
A2-6
A2-6
A1-6
A2-7
A2-7
A1-7
21a-1
21a-2
21a-3
21a-4
21a-5
21a-6
21a-7
21a-8

FIG. 30

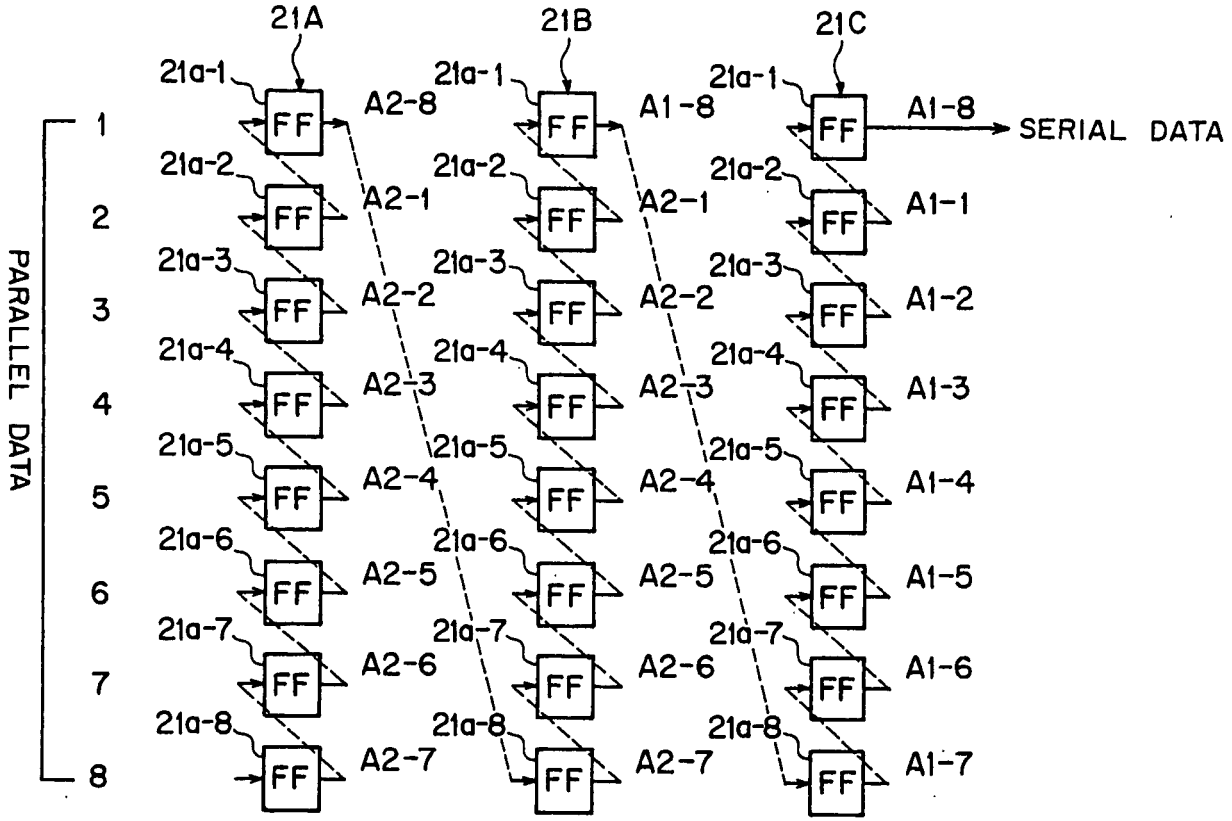

21A
21B
21C
21a-1
21a-2
21a-3
21a-4
21a-5
21a-6
21a-7
21a-8
FF
A2-8
A2-1
A2-2
A2-3
A2-4
A2-5
A2-6
A2-7
A1-8
A1-1
A1-2
A1-3
A1-4
A1-5
A1-6
A1-7
SERIAL DATA
PARALLEL DATA
1
2
3
4
5
6
7
8

FIG.31

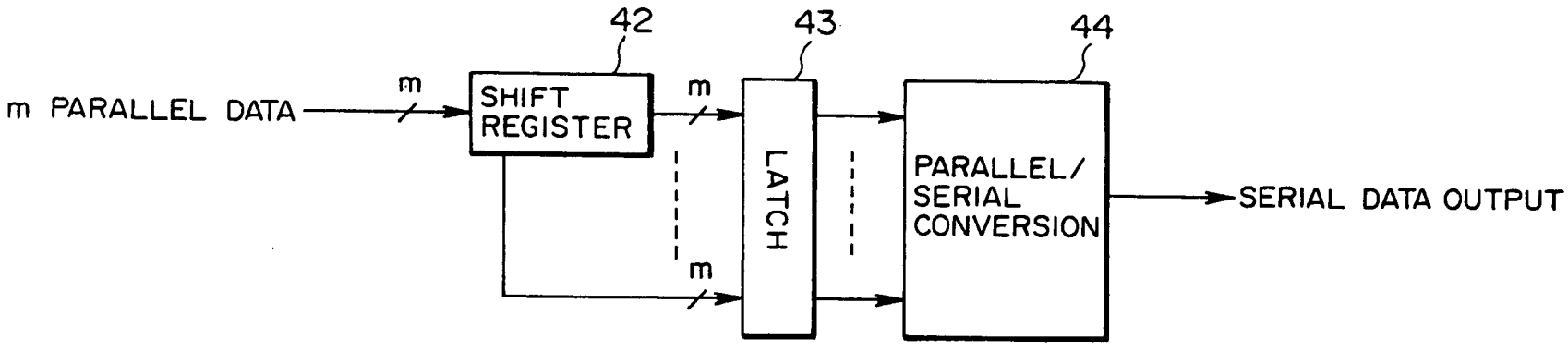

42
43
44
m PARALLEL DATA
m
SHIFT REGISTER
m
m
LATCH
PARALLEL/ SERIAL CONVERSION
SERIAL DATA OUTPUT

FIG.32

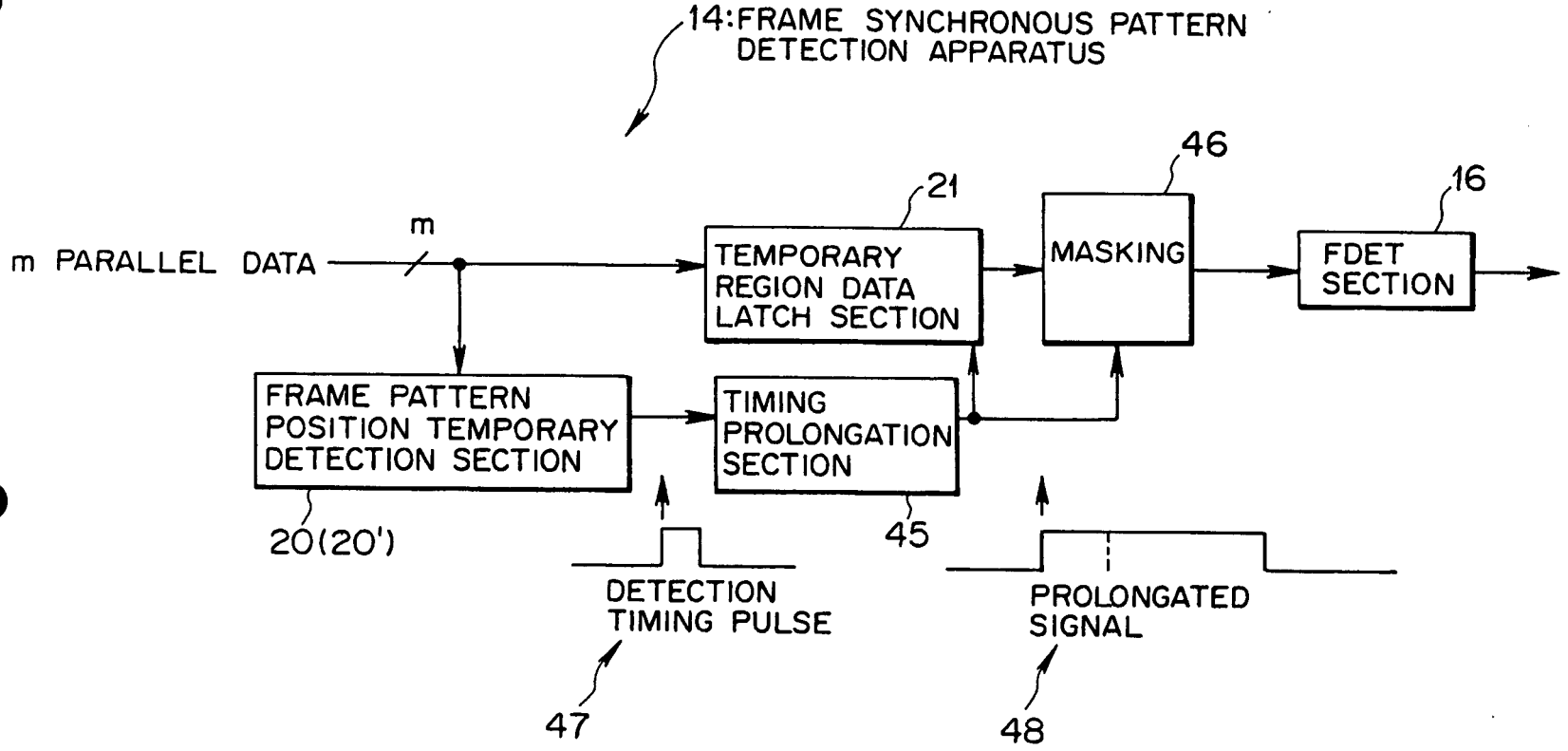

14:FRAME SYNCHRONOUS PATTERN DETECTION APPARATUS
m PARALLEL DATA
m
TEMPORARY REGION DATA LATCH SECTION
21
MASKING
46
FDET SECTION
16
FRAME PATTERN POSITION TEMPORARY DETECTION SECTION
20(20')
TIMING PROLONGATION SECTION
45
DETECTION TIMING PULSE
47
PROLONGATED SIGNAL
48

FIG. 33

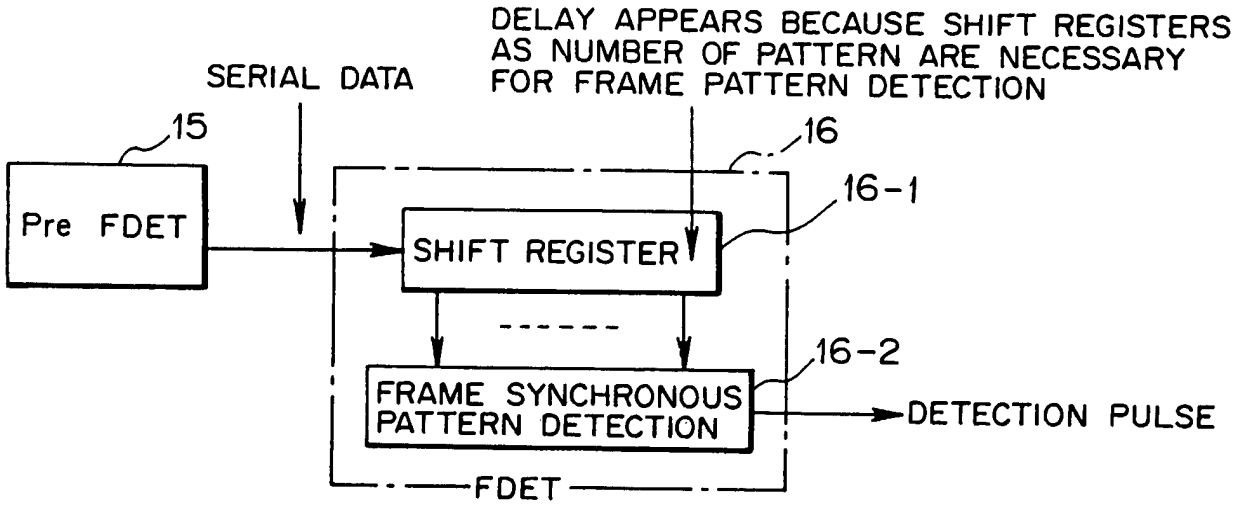

DELAY APPEARS BECAUSE SHIFT REGISTERS AS NUMBER OF PATTERN ARE NECESSARY FOR FRAME PATTERN DETECTION
SERIAL DATA
15
16
16-1
Pre FDET
SHIFT REGISTER
16-2
FRAME SYNCHRONOUS PATTERN DETECTION
DETECTION PULSE
FDET

FIG. 34

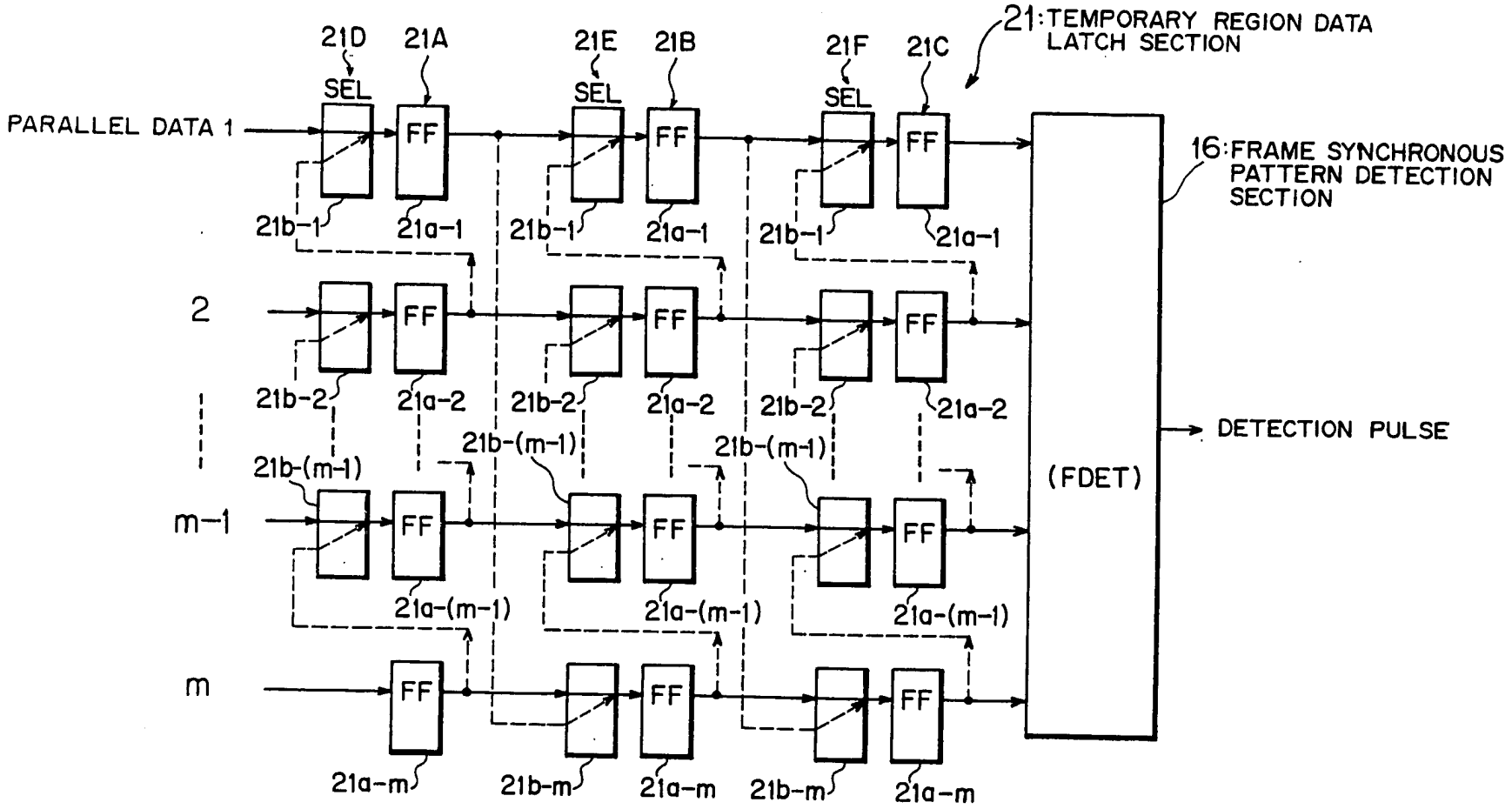

21: TEMPORARY REGION DATA LATCH SECTION
21D
21A
21E
21B
21F
21C
SEL
PARALLEL DATA 1
FF
21b-1
21a-1
2
21b-2
21a-2
m-1
21b-(m-1)
21a-(m-1)
m
21a-m
21b-m
16: FRAME SYNCHRONOUS PATTERN DETECTION SECTION
(FDET)
DETECTION PULSE

FIG. 35

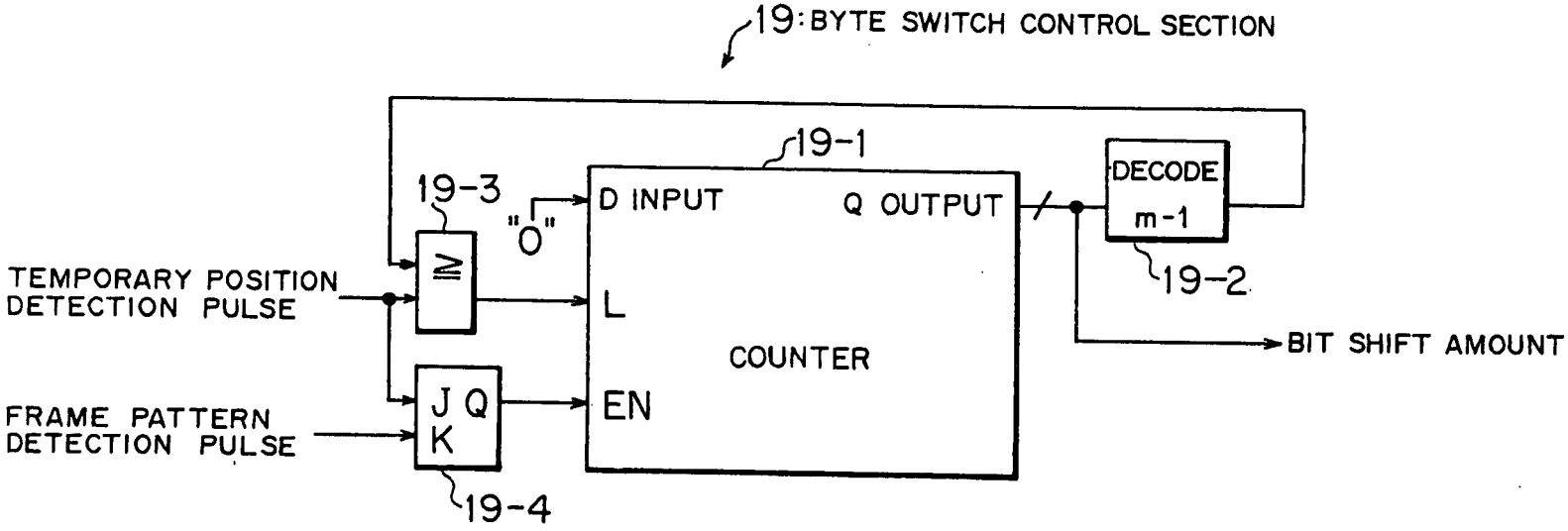

19: BYTE SWITCH CONTROL SECTION
19-1
19-3
"0"
D INPUT
Q OUTPUT
DECODE
m-1
19-2
TEMPORARY POSITION DETECTION PULSE
≧
L
COUNTER
BIT SHIFT AMOUNT
FRAME PATTERN DETECTION PULSE
J Q
K
EN
19-4

FIG. 36(a)

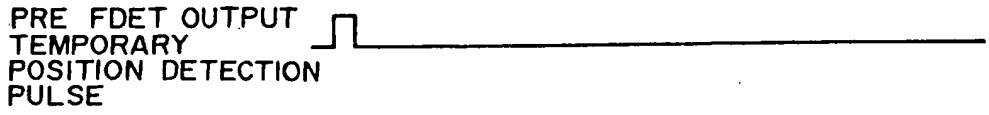


FIG. 36(b)

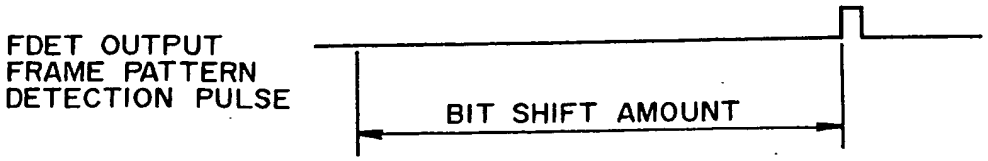


FIG. 37

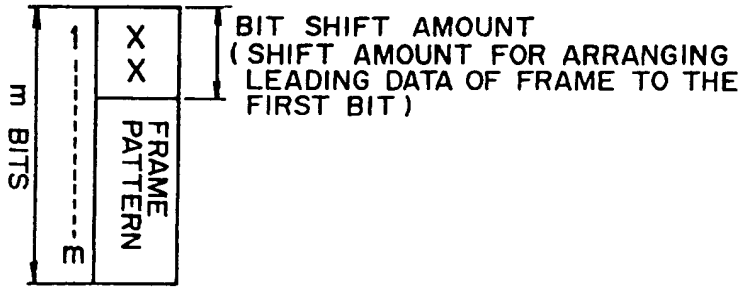


FIG. 38

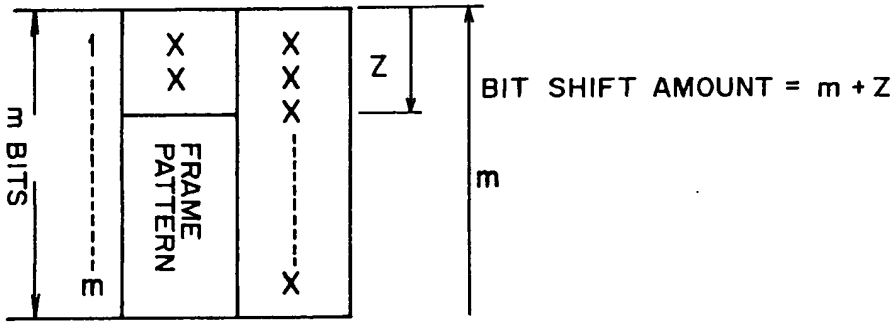


FIG. 39(a) TEMPORARY POSITION DETECTION PULSE

FIG. 39(b) FRAME PATTERN DETECTION PULSE

FIG. 39(c) COUNTER EN (ENABLE)

FIG. 39(d) COUNTER L (LOAD)

FIG. 39(e) COUNTER L VALUE

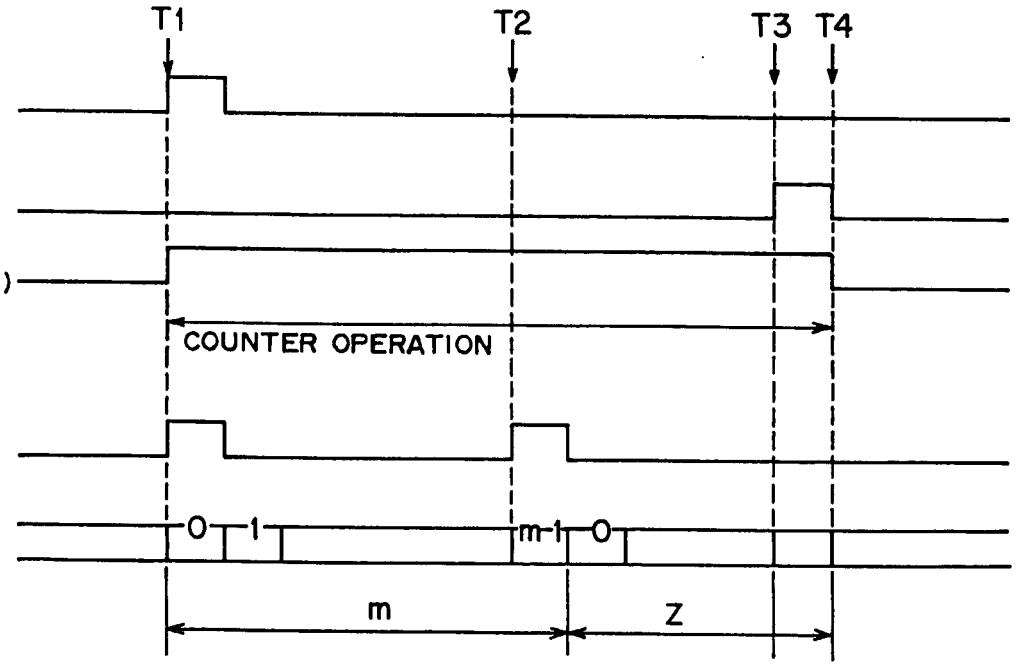


FIG. 40
PRIOR ART

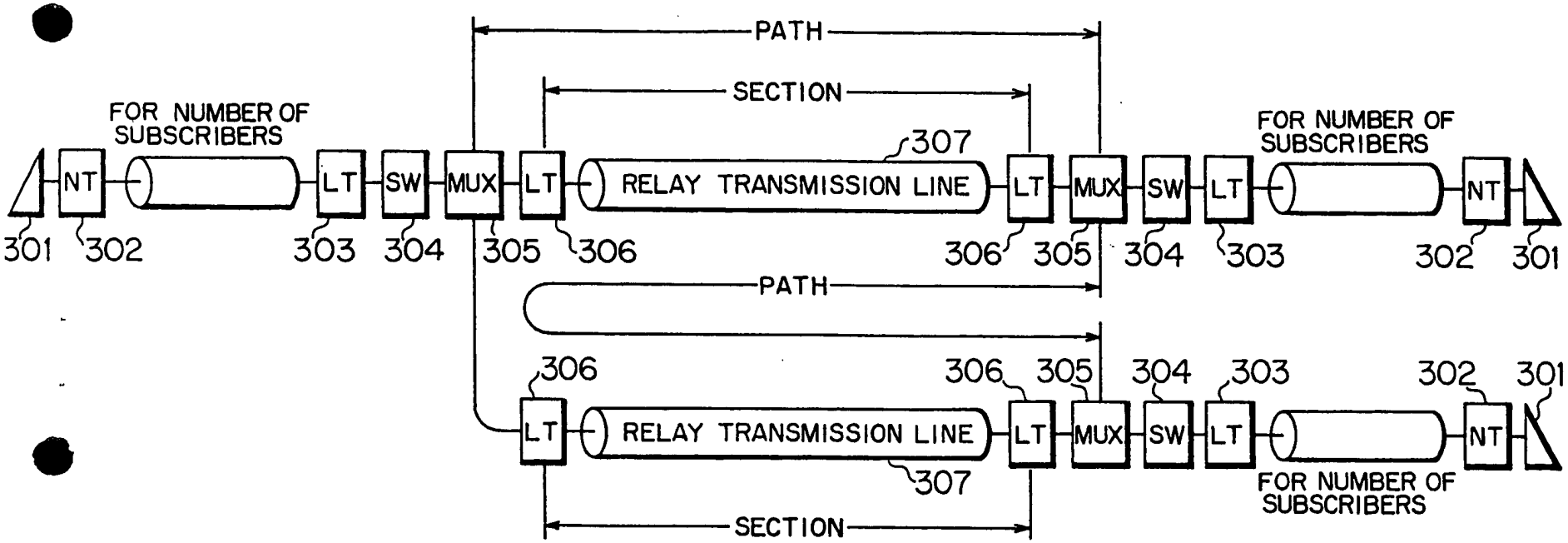


FIG. 41
PRIOR ART

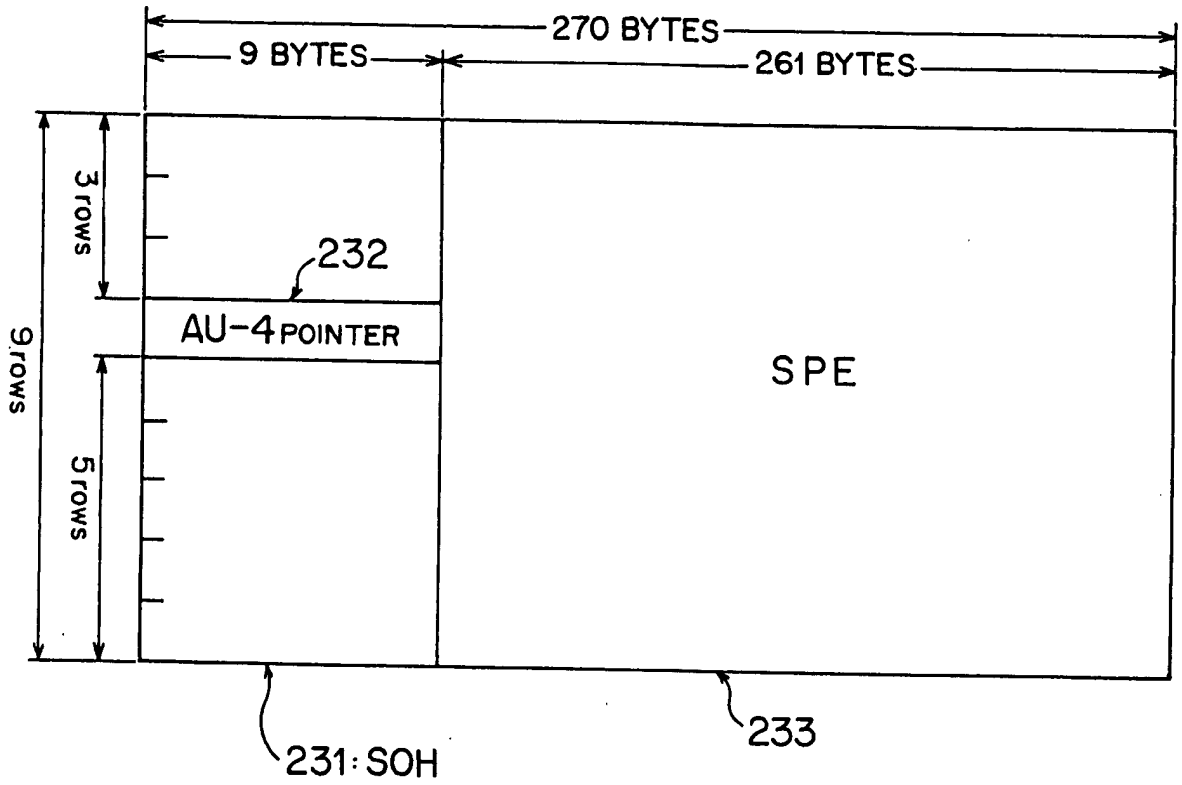


FIG. 42
PRIOR ART

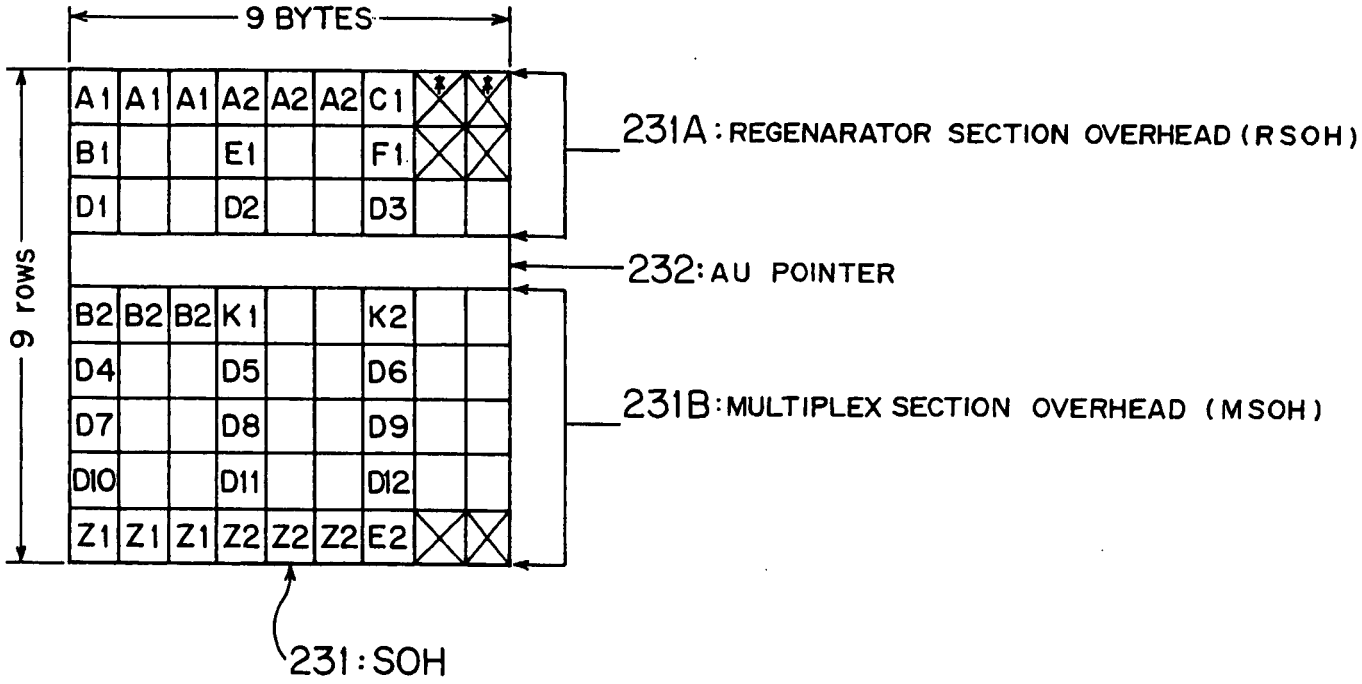


FIG. 43
PRIOR ART

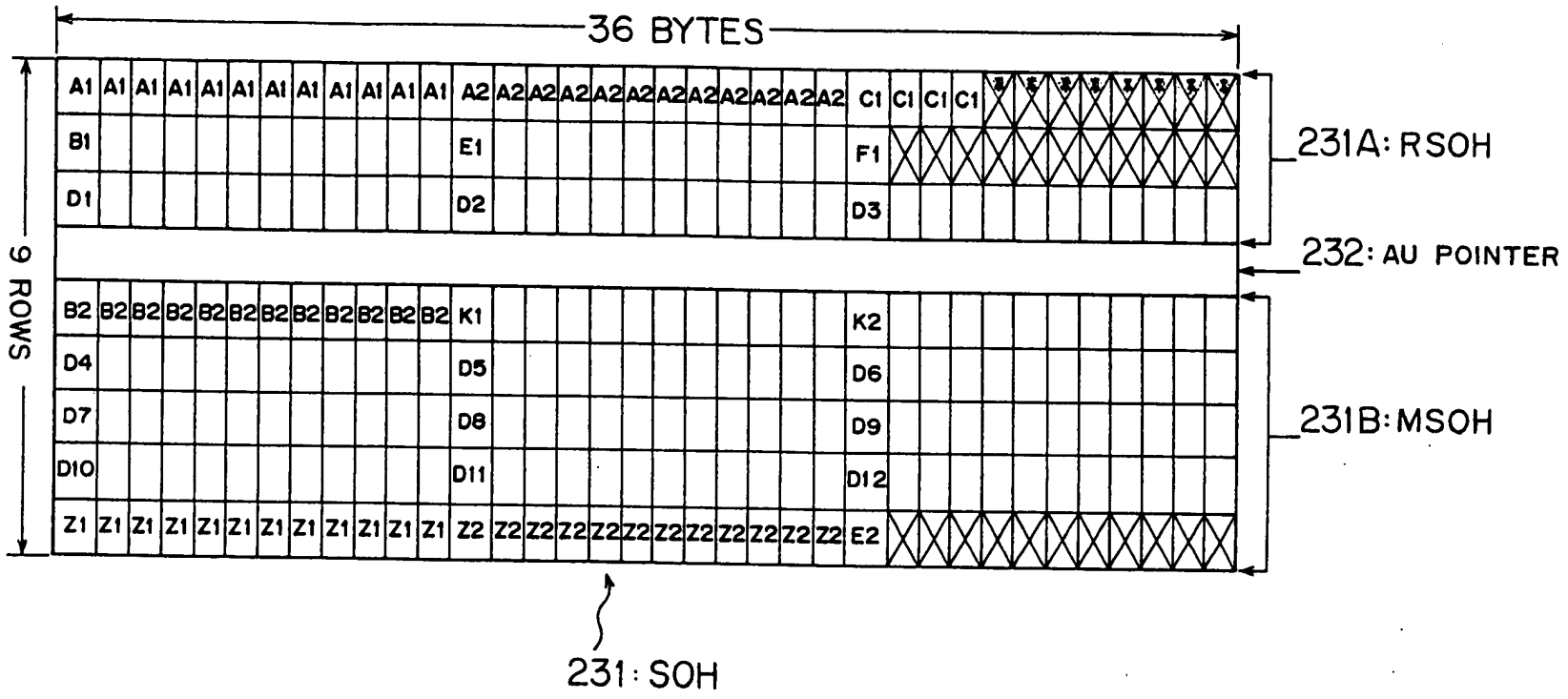


FIG. 44
RELATED ART

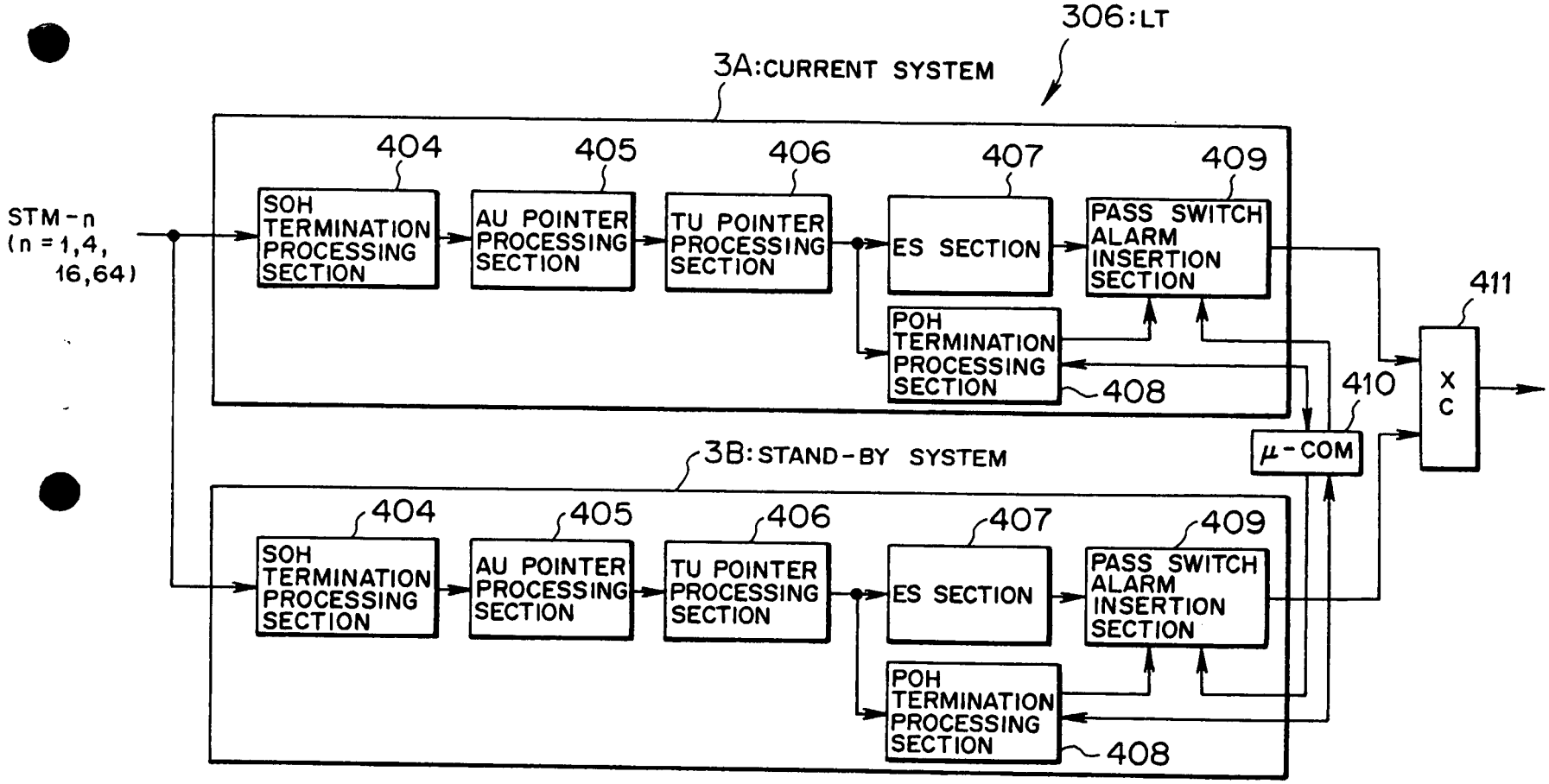


FIG. 45
RELATED ART

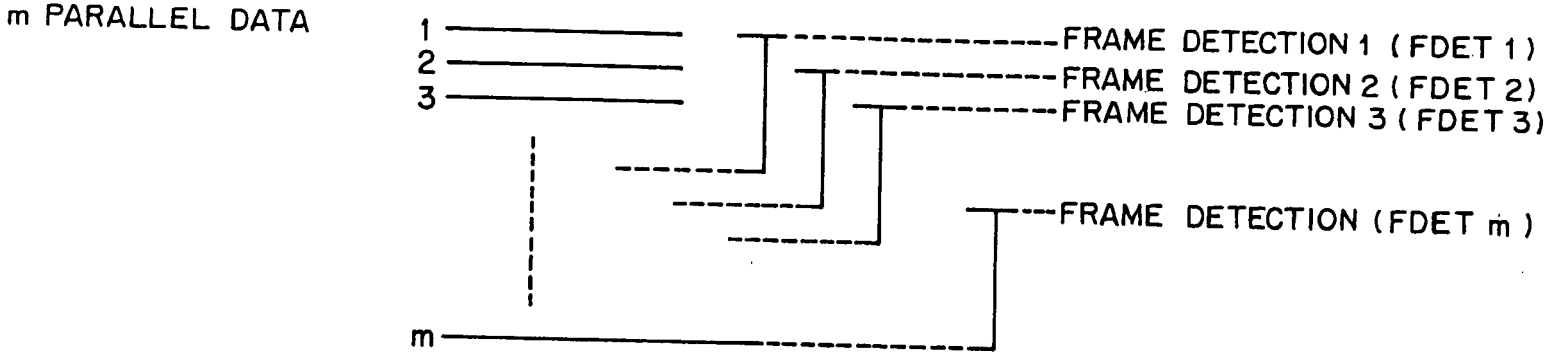


FIG.46
RELATED ART

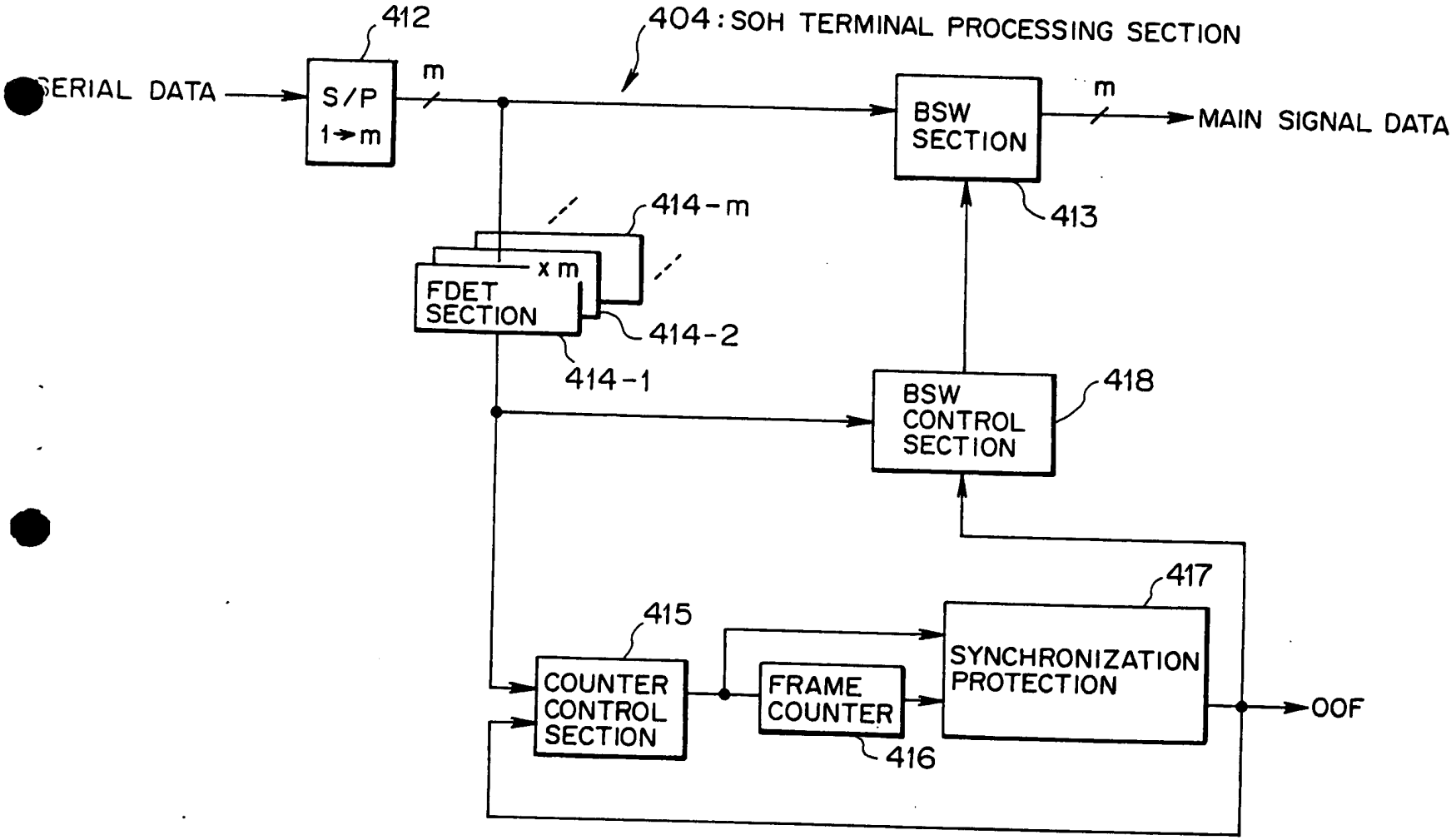


FIG.47
RELATED ART

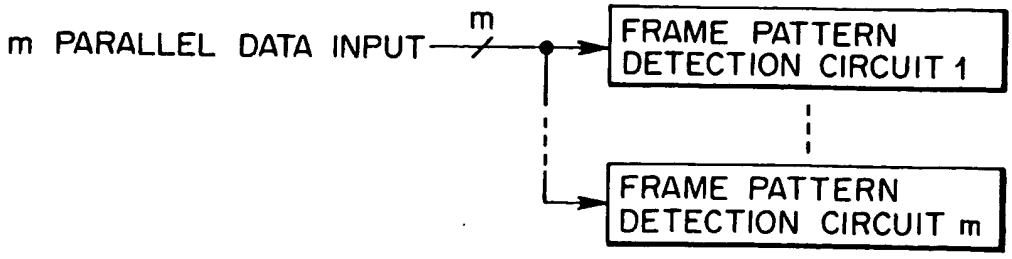



FIG.48
RELATED ART